

1N-91
371985

Mars Micro-Meteorology Station Electronic Design,
Assembly and Test Project

Final Report

NASA-Ames University Consortium

Contract NCC2-5133

Period of Contract:
May 1, 1995 - June 30, 1996

From:

Prof. Robert J. Twiggs, Director
Space Systems Development Laboratory
Durand Rm. 269
Dept. of Aeronautics & Astronautics
Stanford University
Stanford, CA 94305-4035
(415)723-8651 voice
(415)725-3377 fax
Internet: btwiggs@leland.stanford.edu

Graduate Research Assistants:

Seven Merrihew
Brian Engberg
Michael Hicks
Clemens Tillier

To: CAST

Contents

1.0 PROJECT DESCRIPTION	1
1.1 MICRO-MET MISSION	1
1.2 PROJECT CONTEXT	1
1.3 PROJECT PROGRESS	1
2.0 DESIGN DRIVERS	1
2.1 REQUIREMENTS	2
2.1.1 Mission Requirements	2
2.1.2 Project Specific Requirements	4
2.2 PRIMARY HARDWARE DRIVERS	4
2.2.1 Memory	4
2.2.2 Power	5
3.0 IMPLEMENTATION.....	5
3.1 DESIGN PHILOSOPHY	5
3.2 Phase I	6
3.2.1 Components	6
3.2.1.1 MCU	6
3.2.1.2 Timer	6
3.2.2.3 Sensors	7
3.2.2.4 Power	7
3.2.2.5 Comm	7
3.2.3 Operation	7
3.2.3.1 Software	7
3.3 PHASE II [NOT COMPLETED]	8
3.3.1 Components	8
3.3.1.1 MCU	8
3.3.1.2 Timer	8
3.3.1.3 Sensors	8
3.3.1.4 Power	8
3.3.1.5 Comm	8
4.0 LESSONS LEARNED	8
4.1 SOFTWARE DEVELOPMENT ENVIRONMENT	8
4.2 TERMINAL NODE CONTROLLERS	8

APPENDIX I	SOFTWARE STATUS
APPENDIX II	68HC11 DETAILS
APPENDIX III	PHASE I COMPUTER CODE
APPENDIX IV	LiSOC12 Battery Test Report

APPENDICES A-H Supplementary Appendices

1.0 Project Description

1.1 Micro-Met mission

The Micro-Met mission is a micro-meteorological experiment for Mars designed to take globally distributed pressure measurements for at least one martian year. A series of 16 landers equally spaced over the planet's surface will take pressure and temperature data and relay it to investigators on Earth. Measurements will be logged once every hour and transmitted to an orbiter once every thirty days using Mars Balloon Relay protocol. Micro-Met data will aid tremendously in the development and refinement of a global model of Martian weather.

1.2 Project context

The purpose of the work at Stanford was to make a preliminary study of the Micro-Met electronic and power systems. The primary objectives were to verify that the system could operate within the originally budgeted power estimates and to develop a working prototype system. The prototype would initially use whatever hardware fit the functional requirements, and successive prototypes would incorporate increasingly flight-like hardware.

1.3 Project Progress

The Phase I design described in section 3.2 was finished by the end of the project. It used non-flight hardware and communicated by wire, but functioned as desired. Most of the Phase II components were identified and vendors located.

2.0 Design Drivers

This section develops the criteria used for deciding what system architecture will be required and what possible hardware realization to consider.

2.1 Requirements

2.1.1 Mission Requirements

Mars μ -met prototype requirement overview

Flight Hardware	Our Prototype
Mission Requirements:	
1) Record pressure data at desired times 2) Store data 3) Relay data to orbiter 4) Last one Martian year 5) Survive hard-landing loads 6) Bio safety	1) Record pressure data at desired times 2) Store data 3) Relay data to another remote device
Overall Functional Requirements:	
Stay within specified temperature ranges Data integrity Reliable transfer of data from sensors to CPU to comm system Supply reliable power	Data integrity Reliable transfer of data from sensors to CPU to comm system Supply reliable power
CPU:	
Rad hard Not too sophisticated for job Store at least 18 kbits of data Low power operation Standard interface (as specified in RFP, sec. 1.6)	Not too sophisticated for job C programmable Help / expertise readily available for us Store at least 18 kbits of data Low power operation Sufficient interface capabilities
Sensors:	
3 analog pressure sensor inputs, convert to 12 bit 3 temperature compensation sensors, convert to 8 bit Data rate: 25 data points per sol, dumped every 30 days	Same?
Power system:	
Provide surge power when comm is transmitting Survive interplanetary transit time	Provide surge power when comm is transmitting
Comm system:	
Ensure data integrity on uplink (protocol) Low power, high efficiency Compatible with MBR / MGS (see RFP, sec. 1.7)	Ensure data integrity on uplink (protocol) Low power would be nice
Structure:	
Support other components for launch, transfer, entry and landing Proper thermal and electrical properties	Support other components in a 1-G environment Weather proof? (if outside test)

Table 1. Project Requirements

The mission requirements that were relevant to the work done at Stanford include anything to do with the data logging system. Chronologically, these are:

Flight Operations: Battery must retain charge for several months in an interplanetary flight environment

Surface Operations: The system must take pressure and temperature readings 25 times a day. The readings must be processed and stored as a single 12 bit pressure measurement and a single 8 bit

temperature measurement. After 30 days the system must send the stored data to an orbiting relay satellite using Mars Balloon Relay protocol.

The surface operations can be summarized by a simple flow-chart (Figure 1)

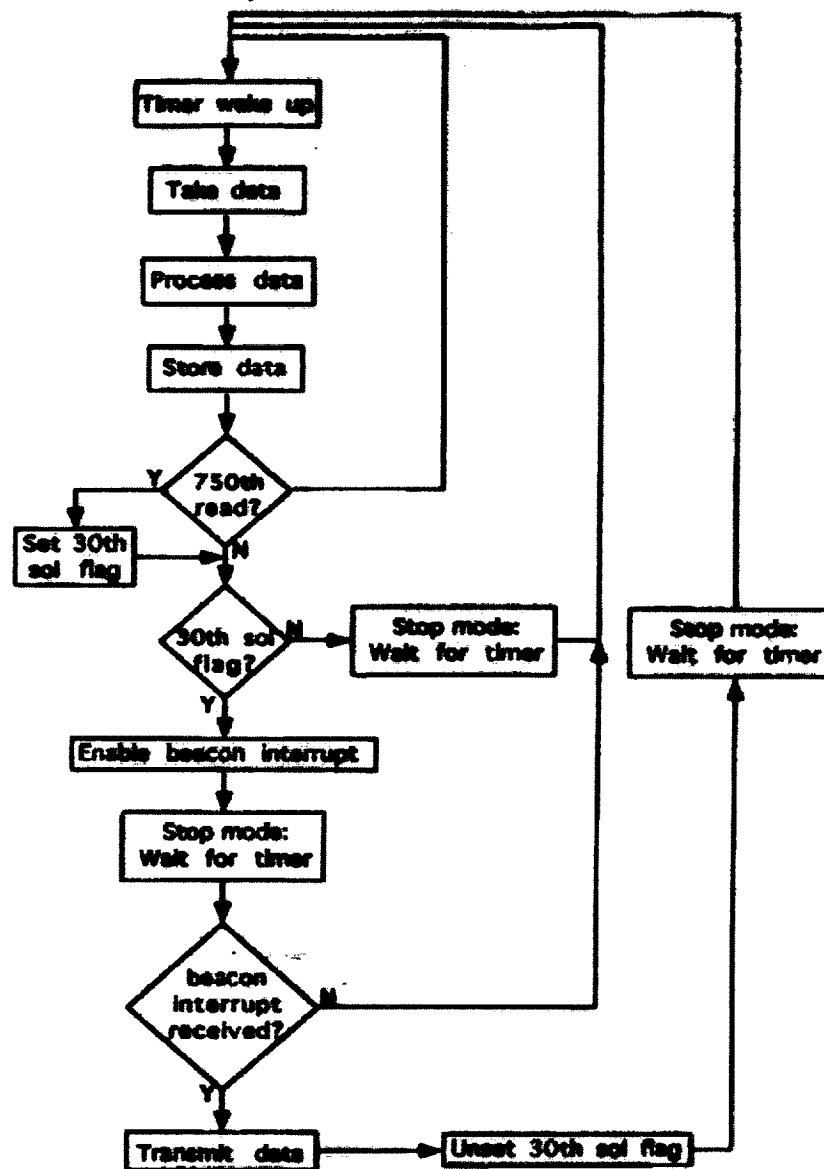


Figure 1. Surface operations flow chart

A timer with a period of an hour initiates operation by turning on the processor. The processor then samples the sensors, processes the data, and stores it in memory.

If this is the 750th read that the processor has made, the processor makes a note of it by setting a flag high. This flag indicates that a month (30 days) of readings have been taken and that it is time to radio the data back to the communications relay orbiter as soon as possible. It will remain high until the communications event has occurred.

Next the processor checks the flag to see if it is high. This is not a redundant measure, because it is possible that the data may not have been transmitted yet because no satellite came into view between the 750th reading and the 1st read of the next month's data. If the flag is not high, there is no need to look for the satellite and the processor goes into stop mode to wait for the next data taking event. If the flag is high the beacon interrupt is enabled.

Enabling the beacon interrupt means that when the radio receiver picks up a beacon signal being put out by the orbiter, it can raise the voltage on one of the external pins of the processor and begin a routine for sending the data. When the interrupt is not enabled, the processor will be insensitive to voltage changes on that pin. Simultaneous to enabling the interrupt, a timer is set up for the communications system. The timer, running independently of the processor, turns on the receiver periodically (probably once a minute). Analog hardware can decode the signal received and, if it is the satellite beacon, activate the processor.

If the processor is activated by the communications system it will run the beacon interrupt service routine automatically upon waking up. This routine simply dumps the data in memory through the transmitter several times while the satellite is still in view. Then the processor deactivates the flag indicating that it was transmit time and goes back to sleep mode, waiting for the next data taking event.

If the processor is not activated by the communications system before the next timer signal initiates a data taking event, the 750th read flag remains high and, after the data taking event, the system goes into the same communications ready mode, waiting to receive a beacon signal.

Thus the majority of the system's life is spent with all components except an hour timer powered down. Every hour the system takes data for a brief moment, then goes back to sleep. Every month the system goes into a mode where it checks for a satellite every few minutes, for probably a day or two, then goes back to normal operations again.

2.1.2 Project Specific Requirements

Limitations on terrestrial radio frequencies, the communications equipment used, and other aspects of the project that diverge from the actual mission requirements are discussed here.

The project prototype will not duplicate all aspects of the flight model. The major divergence will be the communications link, which is limited by the terrestrial environment and available equipment. Mars Balloon Relay (MBR) communications protocol has been baselined for all near future Mars landing missions. The actual MBR frequencies will not be used and communication will be over HAM frequencies between ground locations. Furthermore, the exact MBR protocol will not be used to encode the data.

Instead of the actual communications equipment for the final mission, communication will be over standard amateur radio terminal node controllers running on their own power source while simulating communications event battery loading with dummy load antennae. This will be sufficient to demonstrate the validity of the data logging hardware and the power system.

2.2 Primary Hardware Drivers

2.2.1 Memory

The memory requirements for the mission are driven by the measurements being made, and the strategy for their collection. In turn they drive the selection of the memory hardware and/or processing architecture and have a significant effect on the power requirements. This section discusses these trade-offs.

Each measurement requires 24 bits: 12 bits for the pressure reading, 8 for temperature, and 4 for additional engineering telemetry. The telemetry bits are included in this calculation because conventional memory systems are organized into 8 bit bytes as the base unit. At an absolute minimum, 750 measurements must be stored in memory between uplinks. Thus the memory requirement is 2.25 kilobytes, plus a safety margin to account for delays in establishing the relay uplink, during which data for the next month must continue to be stored.

As described in the implementation section, the 68HC11 family of microprocessors was chosen as the microcontroller for this research project. Except for the MC68HC11A8, on-chip memory in these processors is insufficient. The 68HC811A8, however, includes 8K of EEPROM (electrically

erasable programmable read only memory)¹, which would easily be sufficient for data storage. While EEPROM has the disadvantage of wearing out after 10,000 write cycles, this will not be a factor in a two earth-year mission, which would include only 24 write cycles. Since EEPROM does not require power to maintain bits in memory, it allows the processor to be powered down completely. When being programmed the EEPROM would require a momentary increase in power during the write cycle, which lasts at most 20 ms/byte.

The other option is to use RAM not already built onto the 68HC11 processor. Low power CMOS static RAM is available in an 8K package which has a typical current drain of 1µA at 4.5V supply in standby mode. The current increases to 50 mA during write and read operations.

Comparing the power requirements for a typical monthly cycle, the EEPROM is the better option. If EEPROM is used then memory requires no power at all except during the write and erase sequences, approximately 750x80ms/month. RAM requires at least 12.15 J just to survive in standby mode for a month. EEPROM would have to operate at an additional 40mA of current when it is being written in order to equal RAM energy usage. In order to realize this gain, however, the system must operate with the MCU totally powered down between activities; not feeding the MCU power during the long waits between readings is what makes this option attractive.

Unfortunately, the 68HC811A8 may no longer be in production², and no other production models exist with more than 2K EEPROM built in. Although modular 16-bit motorola microcontrollers can be ordered with specific elements found in the HC11 series, including 8K flash EEPROM³, they do not come with internal charge pumps, which are necessary to produce on-chip voltages for EEPROM programming signals which are higher than the chip supply voltage, and thus they require an external 12V source. Therefore, three memory options exist 1) use static RAM with the associated power increase, 2) develop data compression techniques that would fit saved data into 2K (such as use of only two engineering telemetry bits rather than four), 3) find a different microprocessor with a more optimal on-board memory configuration.

2.2.2 Power

Every electronic component represents a power drain. Although the data logging and transmitting periods represent the most intense use of power in the mission, their frequency is so low that steady state power usage, what the station is doing when it's supposed to be "asleep", is of paramount importance.

OPS mode	Active Components					time in mode per 30 days (s)	percentage
	clock	processor	memory	receiver	transmitter		
sleep	X		TBD			2.70E+06	100
log data	X	X	X			3.00E+03	0.111111
beacon RX on	X	X	X	X		1.60E+02	0.005926
transmit	X	X	X	(X)	X	1.00E+01	0.00037

Table 2. Time systems component spend consuming power

3.0 Implementation

3.1 Design philosophy

The design philosophy of this project is to first develop a functional prototype, then iteratively improve components of the functioning system to be more flight-like. The basic system is introduced here, and then the first and second iteration components and software are detailed.

At the simplest level, the Micro-Met system consists of sensors, a microcontroller unit (MCU), and communications equipment. The sensors take data when the MCU tells them to, the MCU organizes and stores the data, and the communications section sends or receives when commanded by the MCU. This is the essence of a remote data logger, as shown in Figure 1.

¹ MC68HC11 Reference Manual. p 4-4

² Not listed on Motorola web site at http://freeware.aus.sps.mot.com/amcu/sel_guide/index.html

³ Motorola Semiconductor Master Selection Guide, 1994. p 2.5-30

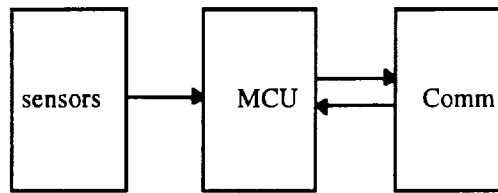


Figure 2. Data flow for elementary data logger

More specifically, in our situation the sensors will be analog pressure and temperature transducers and thus must be converted to digital signals for ease of processing and storage. The communications system will be radio transceiver. In a general sense, the MCU will need to incorporate a processor, memory for data storage, and a timing device to properly sequence operations.

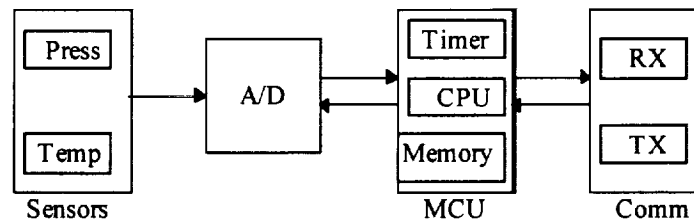


Figure 3. Data flow in Micro-Met hardware components

In the actual implementation then, the main hardware components can be identified and pieced together. A functional model can be achieved first. Then, as development continues, more flight-like hardware can be substituted into the system, iteratively approaching the final design shown in Figure 2.

3.2 Phase I

The first functional prototype accomplishing the following tasks:

The first functional prototype, completed by the end of the 1995 summer quarter, demonstrated all aspects of the Micro-Met function except an actual radio link. It could take measurements, go into standby mode between measurements, and wait until an arbitrary number of samples before responding to a simulated relay satellite signal with a download of data.

3.2.1 Components

The phase I components were, for the most part, rather crude yet sufficient to demonstrate functionality.

3.2.1.1 MCU

The microcontroller was an F68HC11FN made for New Micros Inc. by Motorola. A standard, 68HC11 processor, it was mounted in a board provided by NMI complete with 12 bit A/D features and additional memory on the address bus. Programming (code included in Appendix) was done using the SmallC compiler and the freeware assembler supplied with the board.

3.2.1.2 Timer

The timer was the least flight-like component. It consisted of a 555 timer set up as an oscillator feeding into the bottom stage of an 8bit binary counter (4020B). Different periods could be selected by running the output of later stages to an edge trigger circuit constructed from nand gates. The edge-trigger was calibrated by varying resistance and capacitance attached to its output to provide a short enough pulse to be seen as a single interrupt at the 68HC11 XIRQ and IRQ ports. The

XIRQ and IRQ ports were used to indicate a satellite ready to receive and to wake up the CPU when in sleep mode, respectively.

3.2.2.3 Sensors

LM35 temperature sensors were used for the 8-bit temperature inputs. Simple potentiometers to provide variable voltages were used to simulate the pressure sensors.

3.2.2.4 Power

Power for phase I was simply provided by a variable voltage supply. While desired operation of the CMOS 68HC11 is at just above 3V for power efficiency, power was kept at 4.5V because the voltage regulator built into the NMI board won't operate that at 3V.

3.2.2.5 Comm

Communication between the NMI and the "ground station", a PC, went through two KPC-3 Terminal Node Controllers (TNC's) connected with null modem cable to simulate the radio link. Data from the MCU were sent out the Serial Communication Interface (SCI) into an RS232 connection to the first TNC. Instead of connecting to a radio transmitter, the output of TNC1 was connected directly to the radio input of TNC2 (where a radio receiver normally is attached). TNC2 was linked via RS232 cable to a computer running PROCOMM, a terminal emulation software package.

3.2.3 Operation

Fleshing out the functional diagram with the parts described above, the system now looks like

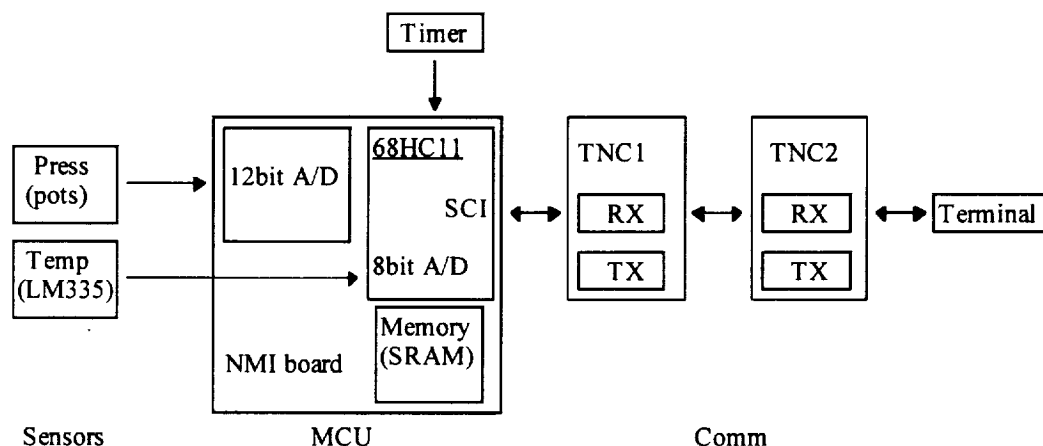


Figure 4. Phase I system block diagram

3.2.3.1 Software

Coding for the MCU was done using a combination of C and 68HC11 assembly. The overall system was written in C while many of the specific operations such as A/D conversions and interrupt routines were written in assembly and inserted as modules. Code was written in a DOS environment with the a standard DOS editor. The NMI board came with a custom compiler, called SmallC, for converting C code to assembly commands. A second shareware compiler, called AS11, was used to convert the assembly code to machine code understandable by the 68HC11. MAXTALK, A terminal program, was used to talk to a BUFFALO (Bit User Fast Friendly Aid to Logical Operation) monitor EPROM plugged into the NMI board. The Buffalo chip is a program resident in 68HC11 ROM which aids in interfacing with and debugging programs. Using the terminal and the monitor program, the machine code was downloaded to the NMI and run.

The software is organized hierarchically. A main program establishes the behaviour of two interrupt service routines, the first of which responds to a timer with a standard data taking event, the second of which responds to a simulated beacon by initiating a communication event. The basic flow

of the program is described in detail in the *Mission Requirements* section of this report. The status of the different subroutines is described in Appendix A. Additional information about assembly level programming of the 68HC11 processor is presented in Appendix B. The actual code for Phase I is included in Appendix C.

3.3 Phase II [Not Completed]

3.3.1 Components

A more integrated package without the New Micros board overhead is possible. Elimination of all components on the NMI board that are not relevant to the Micro-Met mission can lead to significant space savings and a package smaller by a factor of two to three. A commercially available "BotBoard", which has only the 68HC11, a reset button, and a few necessary crystals, capacitors, and resistors, is 2" x 2".

3.3.1.1 MCU

same as Phase I

3.3.1.2 Timer

The cobbled together Phase I timer can be replaced by a single chip, the ICM7170. This chip can provide periodic interrupts at 1 minute, 1 hour, and 1 day intervals and requires only about 2 μ A for normal operation. The ICM7170 is manufactured by Harris Semiconductor. Detailed information on this timer is available at: <http://www.semi.harris.com/datasheets/micro/icm7170/icm7170.pdf>

3.3.1.3 Sensors

same as Phase I

3.3.1.4 Power

Lithium Thionyl Chloride batteries

3.3.1.5 Comm

KPC-3 TNC's will be used as in Phase I. However, the null modem cable will be replaced by an actual radio link established between a Yaesu FT-350 HT (handheld transmitter), which is a small portable amateur radio, and an established ground station, which is located at Stanford and operated by the Space Systems Development Lab.

4.0 Lessons Learned

4.1 Software Development Environment

In the course of work on the code for the 68HC11, and in consultation with other Stanford workers who have done development on the same platform, it was determined that the SMALLC environment was not ideal for this work. Almost any other commercially available compilers are more user friendly, faster, and have better linkers. SMALLC includes several elementary flaws making it unable to fully implement all ANSI C commands.

4.2 Terminal Node Controllers

The terminal node controllers were adopted into the design as an interface to the radio link so that element of the system could be made functional, if not flight-like. Interfacing to the TNC's entailed a great deal of software overhead that is very system specific and that will not be used in the final system. A majority of hold-ups and software/hardware problems were associated with this link. Perhaps in future work more flight-like components could be acquired and interfaced to so that the specific work necessary to integrate the comm system is not wasted.

Appendix I

Micromet Software Status (23 August 95)

Most of the Micromet Prototype software is now implemented in C. The biggest problem to be resolved is the processor interrupts.

Top-level operation:

File: MICROMET.C. This just makes calls to all the functions below. It's based around two interrupt service routines (ISRs). The first ISR (triggered by the IRQ interrupt) will take a sample, process it, and store it. The second ISR (triggered by XIRQ) will transmit the data to the ground station. The processor spends most of its time in STOP mode, with the clock disabled. The overall system doesn't work yet, due to complex intricacies of the interrupt setup.

Scanning data from the ADCs:

File: READ_AD.C. This was written around an assembly routine put together by Mike. Three 8-bit ACD and three 12-bit ADC channels are read and stored into the HC11's on-chip RAM. Debugged, works.

Doing a complete read for a sample:

File: READATA.C. Makes however many ADC scans requested, and stores the data in buffers in the data segment of memory. Makes use of a bitshift function written in assembly. Debugged, works.

Processing the sample:

File: PROCESSD.C. For now, this isn't very sophisticated. It just averages the readings to come up with two numbers: temperature and pressure. This can be fleshed out at a later date to make more sophisticated checks on the data; 4 bits are provided in each sample to store flags. Debugged, works.

Storing the sample:

File: STORDATA.C. This just shoves the two numbers into the long-term memory block, and keeps track of where it should put the next sample. Debugged, works.

Incrementing the sample counter, and activating the receiver interrupt:

File: INCR.C. This keeps track of how many samples were taken. If the number exceeds a predetermined total, steps are taken to start listening for the beacon. (i.e. do a hardware enable of the XIRQ pin, by powering up the receiver). For now, this just increments the sample counter; we don't have a receiver yet.

Transmitting the data:

File: TRANSMIT.C. This reads memory and shoves it out to the serial port. Since we're using TNCs with a terminal program, we can't directly transmit binary data. We are forced to do something akin to UUencoding, by transforming the binary data in memory to its ASCII representation in hexadecimal. The data is then piped out the serial port as a text file, after appropriate formatting for the TNC. The function does not work yet, since it makes use of several other functions that haven't been integrated.

Converting data to hex ASCII:

Files: ATOHA.C, ITOHA.C. The first takes a character (1 byte) and converts it into a hex representation. For example, a binary representation of 'A' (01000001) gets read out as '41'. The second function does much the same thing, but with an integer (2 bytes). By doing this conversion, we double the amount of information to be transmitted. Both functions work, but they're not bug free.

Transmitting through the TNC:

File: TNC_SEND.C. This packages a string to be sent out, by putting the appropriate control characters before and after the message. Debugged, works.

Flushing the memory for a new sampling run:

File: FLUSH.C. This goes through the data storage segment, and reorganizes everything. Data that was taken while waiting for the beacon is moved to the bottom of the segment, and the sample counter is updated. Not debugged.

Appendix II

WHAT WE NEED FROM THE μ -Met MCU AND HOW WE WILL IMPLEMENT IT

Begun: MTH 7/7/95

Last modified: MTH 8/10/95

List of required capabilities addressed

A/D CAPABILITIES

12-BIT PRESSURE READINGS

MUX control of pressure signals

A/D chip

8-BIT TEMPERATURE READINGS

STORE READ DATA FOR PROCESSING

PROCESS DATA

STORE PROCESSED DATA IN LONG-TERM MEMORY

EEPROM

EXTERNAL RAM

8k x 8 bit static ram chip

INTEGRATION OF RAM INTO ADDRESSABLE MEMORY

Expanded mode

Address and data bus control

TIME UNTIL NEXT READING

EXTERNAL TIMER

POWER CONTROL

POWER CONSERVATION MEASURES ON 68HC11

STOP mode for MCU

Power down A/D converter

Clock speed

CONTROL OF OTHER IC'S

BEACON RECEIVER INTERFACE

INTERFACE TO TNC

A/D Capabilities

12-bit pressure readings

The pressure readings require 12 bit accuracy (that's 0.0488% of the full scale measurement for the decimally inclined) which means we will need to use a separate chip to do the conversions as the 68HC11 only does 8-bit accurate conversions.

MUX control of pressure signals

A/D chips in the catalogs that I've seen so far only have one input, thus we will probably need to control our polling of the pressure sensors with two control lines running to a 4 to 1 MUX before the signals get to the A/D. We have bought a dual 4-input analog MUX from Fry's for this purpose. The chip number is MC14052 and the pin-out appears in the Motorola CMOS Logic Data book on page 6-133.

A/D chip

There is a 12-bit A/D converter with sample and hold available in the Digi-Key catalog for \$17.88. The chip puts out 12 bits from parallel output pins. Once we use ports B and C on the 68HC11 to expand our available memory (see below), we probably won't have enough pins remaining to read this in all at one time. The answer is probably to separate the 12 bits into two sets of 8 lines (one with the top four held to 0) attached to the data bus by two buffers which can be addressed by the address bus as two consecutive bytes somewhere in memory. Also, we will require one line from the 68HC11 to the A/D to activate its sample and hold.

Thus our scheme for operating the A/D will be to give it a signal for sample and hold by writing into one of the output port registers, then read it into a double-byte register from its "memory address".

Available from Analog Devices:

AD7880: -40° to +85° C, 0 to 5V range, 5V power supply!!!

p 2-611

However, they don't sell small quantities and laughed at the idea of buying just two.

This chip is available from Allied Electronics in our area (1-800-262-5645) for \$23.11

8-bit temperature readings

The onboard A/D converter will resolve to 8-bits an analog voltage between the voltages set to pins VRL and VRH. To use the A/D converter we must first turn it on by setting the ADPU (A/D power up) bit (7) of the OPTION register (\$1039) to 1.

OPTION	ADPU	CSEL	IRQE	DLY	CME	FCME	CR1	CR0
\$1039	1	-	-	-	-	-	-	-

To initiate a conversion sequence we must write to the ADCTL register (\$1030). This register has bits to control the way the A/D channels are scanned and where results are returned. If we set the register to

ADCTL	CCF	blank	SCAN	MULT	CD	CC	CB	CA
\$1030	0	0	0	1	0	0	0	0

the processor will scan the first four A/D (port E) pins and return the results to the registers ADR1-ADR4 in 128 E-clock cycles. This is probably the way we want to go, simply waiting until the results are read, then dumping this to a table in working RAM.

Notes: 1) If we set the E-clock speed below 750 kHz (to conserve power, say), we will need to select the on-chip RC oscillator to run the A/D by setting the CSEL (clock select) control bit in the OPTION register. In that case we will need to pay attention to the CCF (conversion complete flag) as the conversion won't take exactly the known 34 E-clock cycles as it does in normal operation. Also, since the RC oscillator will be asynchronous with the E-clock more noise will be induced in the measurement if the RC option is used.

2) Is Catling taking care of the temperature sensors for the prototype or do we need to find thermocouples and make a lookup table inside the processor to get very accurate voltage to temperature conversion (or will this data just be sent back raw then converted back on Earth)? If so, what range do we want the prototype to sample?

Store read data for processing

The data for the 12-bit conversions will be collected by a LDY command addressed to the position in memory space we wire the A/D converter into. The AD7880 has an option to facilitate connection to an 8-bit data bus.

The data from the 8-bit conversions will be read from the ADR1-ADR4 (\$1031-\$1034) and transferred via registers A and B to working memory.

To time our scans of the A/D ports so that we do one every 0.5 seconds we will use the programmable timer. By enabling the TOI (timer overflow interrupt) bit in the TMSK2 register, the TOF (timer overflow flag) will cause a jump to interrupt subrouting at \$FFDE. From there we branch to a subroutine that counts timer overflows and tells us when we have passed 0.5 seconds.

Note: 1) Since the timing of A/D polls is arbitrary, we can probably make the time the closest integer number of overflows to 0.5 seconds rather than timing *exactly* 0.5 seconds

2) If we can take 16 rather than 20 measurements the averaging routine becomes merely a sum and bit shift right operation.

Process data

Data will be processed via a simple algorithm to be developed in C code then cross-compiled to machine language source and down-loaded to the NMI board. The basic function of the program will be to analyze first 20 samples taken over 10 seconds from each sensor individually. A measure of noisiness will be acquired by comparing the average to the standard deviation. Then the averages of each sensor will be averaged together. Individual sensor averages will be compared to the average of each the group and major discrepancies will be noted in engineering telemetry and eliminated from the processed data.

Store processed data in long-term memory

The processed data must be saved to another location in memory where there is more room and which will not be lost if the processor is shut down to conserve power. Although the 256 to 512 bytes RAM built into the 68HC11 (depending on which version we buy) can be kept intact by a separate voltage supply when the rest of the chip is powered down, at least 1.8K data will be stored over a 30 sol period, for which internal RAM is insufficient.

Options for storing the data include onboard EEPROM (electrically erasable programmable read only memory) and external static RAM. The EEPROM information is not lost when power is removed, and the RAM can be kept alive with minimal power.

EEPROM

8K EEPROM is available on the MC68HC11A8 board (maybe), and the next best is the 2K available on the MC68HC11E2. Although pending formalization of the data to be stored for transmission, we know that we'll need 2 bytes pressure data plus 1 byte temperature x 25 readings/sol x 30 sols/cycle pressure cycle. Thus 2.25K is necessary, plus station identification and other protocol. So only the E2 remains an option.

The limitation of EEPROM is that it's bits can only be written from 0 to 1 to 0 again about 10,000 times. Fortunately, if we maintain a standard table organization, a given bit in our EEPROM will only be written to something like 100 times on a 5 earth year mission.

Note: The same need for an RC oscillator to drive the voltage pump for EEPROM writes and erases as in the A/D situation occur when the E-clock speed is very low.

External RAM

The 68HC11 has 64K of addressable memory space, only a fraction of which actually connects to anywhere on the chip. In extended mode the 68HC11 can use ports B and C as address and data buses for communicating to external memory and other devices.

8k x 8 bit static ram chip

We have bought an 8k x 8 bit RAM from Jameco for \$2.95. Hopefully it comes with a pin-out.

Integration of RAM into addressable memory

Expanded mode

To set the 68HC11 to treat ports B and C as extended memory busses the external pins MODB and MODA both need to be set to high.

Address and data bus control

Time until next reading

There are two software commands that put the 68HC11 into a low power consumption mode, WAI (wait for interrupt) and STOP (stop processor clock). WAI will reduce current use to around 10 mA and waits for any external or internal interrupts. STOP will reduce current use to 50 μ A and waits for an external interrupt appearing on the XIRQ or IRQ pins to turn on again.

However, the onboard timer overflows on the order of a second and requires an interrupt routine to count the number of overflows to time longer events like the hour-long wait we want. Thus the WAI command would have to be interrupted thousands of times an hour.

This means that we will probably use the STOP command, which will require an external timing device to ping the XIRQ pin and wake the MCU up again.

External timer

To do the timing we have bought two different chips to experiment with. 1) 24 hour 50Hz 6digit with alarm (Jameco \$1.25) and 2) 12 hour 60Hz 6 digit with alarm (Jameco \$1.25). We should be able to set the alarms on these to go off at the exact minute we want them to which will be convenient for testing purposes when we want shorter than hour long intervals. We may find a chip that is more tailor made for our purposes later on.

Power control

Power conservation measures on 68HC11

STOP mode for MCU

As discussed earlier, this can reduce power use to 50 μ A

Power down A/D converter

Once the program is done with the A/D conversions and is moving on to process the collected data, the A/D can be powered down by setting the ADPU bit in the OPTION register to 0 again.

Clock speed

CMOS power use is strongly influenced by the frequency of signals used, and dramatic power savings can be gained by running internal frequencies as low as possible. A variety of clocks on the 68HC11 are driven at different multiple rates from the main oscillator. We can set these to be as slow as possible. It is even possible to run the MCU through it's EXTAL pins with an external oscillator running off a lower frequency crystal than that built into the 68HC11. This may be implemented on our prototype after all other functionality has been accomplished.

Control of other IC's

During the waiting periods, all other IC's besides the clock can be turned off as well to further conserve power.

Beacon receiver interface

When we decide on the transceiver to be used we will need to determine what sort of output abilities it has. We can either run output of the receiver directly our own hardware for detecting the beacon signal, or have output running to the TNC where the MCU polls to look for it.

Interface to TNC

We have to find a TNC to use.

Appendix III

Micromet Code

The first program following is Micromet.C, designed to be the backbone of the final micromet software. The basic implementation can be easily seen here.

The following program is the actual main program used for the final Phase I design. It follows the same philosophy with a few modifications specific to the Phase I hardware, and is not as well documented. All the C code included into this program follows in hardcopy. The standard C libraries are not printed out. All the software developed during the project is available on the disk titled "Micro-Met Code"

```

/* File: micromet.c
 * Written by Clem Tillier 06 August 95
 * -----
 * This is the top-level code for the 68HC11-based micromet prototype.
 * The structure of the program is somewhat unusual, since the default
 * state of the processor is STOP mode, with the clock turned off. The
 * meat of the program is in two interrupt service routines. The first
 * is invoked when the sample timer goes off, and basically takes the
 * hourly sample of data. The second ISR is invoked when the beacon is
 * heard, and deals with transmitting the data.
 * -----
 */

#code 0xD000
#data 0xC000

#include "tncsend.c"

#define MAX_SAMPLES 750 /* Max number of samples between transmits */
#define TRUE 1          /* Handy boolean definitions */
#define FALSE 0

int sample = 0;          /* Global sample counter */

int temp1[16];           /* Global data arrays, used */
int temp2[16];           /* to store ADC readings */
int temp3[16];
int pres1[16];
int pres2[16];
int pres3[16];

main()
{
    Initialize();
    Sleep();
}

/* -----
 * This external interrupt routine simply organizes a sampling run. Data
 * is read from the A/D, processed, and stored in RAM. The sample counter
 * is incremented. The interrupt timer is reset, and the processor is
 * flatlined. If the sample counter reaches the max number of samples,
 * the ArmReceiver turns on the receiver, which does a hardware enable of
 * the xirq interrupt.
 * -----
 */

interrupt irq() {
    ReadData();
    ProcessData();
    StoreData();
}

```

```
sample++;  
ArmReceiver();  
ResetTimer();
```

```
/* -----  
* This interrupt service routine takes care of transmitting data to the  
* orbiter when the beacon is heard. It turns off the beacon receiver,  
* transmits data from MAX_SAMPLES sampling runs, resets the sample  
* counter to the appropriate value, reconfigures the data in memory,  
* and flatlines the processor.  
* -----  
*/
```

```
interrupt xirq() {  
    CloseEars();  
    Transmit();  
    ResetSample();  
    FlushData();  
}
```

```
/* Micromet test code for Phase I hardware */
/* Demonstrates functionality using interrupts as specified in MICROMET.C */
```

```
#code 0xC900
#data 0xC800
```

```
#define BEGINSTOR 0xC000
#define ENDSTOR 0xC7DF
#define MAXSAMPLE 16
#define NUMREAD 16
#define MESSAGE 0xC7F0
#define SAMP_ADDR 0xC7E2
#define MEM_PTR 0xC7E0
#define MAX_BUFF 10
#define TRUE 1
#define FALSE 0
```

```
#include <forth.k>
#include <stdio.h>
#include "scan_ad.c"
#include "readdata.c"
#include "bitchift.c"
#include "processd.c"
#include "stordata.c"
#include <fopen.c>
#include <ser_out.c>
#include <ser_in.c>
#include <fputc.c>
#include <fputs.c>
#include "tnc_send.c"
#include "readcomm.c"
#include "parsemsg.c"
#include "transmit.c"
#include "itoha.c"
#include "atoha.c"
#include "strlen.c"
#include "reverse.c"
#include "incr.c"
#include "flush.c"
#include "rtson.c"
#include "rtsoff.c"
#include "openears.c"
```

```
char t1[NUMREAD];
char t2[NUMREAD];
char t3[NUMREAD];
int p1[NUMREAD];
int p2[NUMREAD];
int p3[NUMREAD];
```

```
char* memptr;
FILE stdout;
```

```
char inBuffer[MAX_BUFF];
```

```
main()
```

```
    stdout = fopen(SER_out);  
    poke(MEM_PTR, BEGINSTOR); /* initialize mem pointer */  
    poke(SAMP_ADDR, 0);      /* initialize sample counter */
```

```
/* Enable STOP */
```

```
#asm  
LDAA  #$00  
TAP  
#endasm
```

```
/* Turn off RTS */
```

```
RTSoff();
```

```
e_int();
```

```
#asm  
SEI  
#endasm
```

```
/* this trick disables IRQ on startup */
```

```
/* Go to sleep and stay there until interrupts */
```

```
#asm  
LP STOP  
BRA LP  
SWI  
#endasm  
}
```

```
interrupt xirq() {  
    ReadData(t1,t2,t3,p1,p2,p3);  
    ProcessData(t1,t2,t3,p1,p2,p3);  
    StoreData();  
    Increment();  
    fputs("Done taking sample...\n", stdout);  
    OpenEars(stdout);  
}
```

```
interrupt irq() {  
    fputs("Attempting to send...\n", stdout);  
    RTSon();  
    ReadComm(inBuffer);  
    if (ParseMessage(inBuffer)) {  
        Transmit(stdout);  
        FlushData();  
        #asm  
        SEI  
        #endasm /* if successful, stop further attempts */  
    }  
}
```

```
RTSoff();
```

```
}
```

```
/* Set interrupt routine vectors */
```

```
#asm
```

```
ORG    $00EE
```

```
JMP    $D78C
```

```
JMP    $D6F1
```

```
ORG    $D7F9
```

```
#endasm
```

```

/* File: SCAN_AD.C
 * written by MHicks and ctillier
 * -----
 * Runs through the appropriate A/D channels and dumps the results
 * into low ram (this is the part implemented in assembly). The C code
 * then picks up the data there and stores it in the right arrays,
 * passed in by reference. (I found no better way to do this... no
 * globals, no structs, no two-dimensional arrays...)
 * -----
 */

```

```

ScanAD(i,b1,b2,b3,b4,b5,b6)

```

```

int i;
char *b1;
char *b2;
char *b3;
int *b4;
int *b5;
int *b6;

```

```

{
#asm
 * Program for scanning and storing 1 sensor sweep
 * MHicks      8/7/95

```

```

 * This program executes the data gathering function of the processor
 * and should be called whenever the timer interrupt wakes the MCU up

```

```

*****
 * Set some constants *
*****

```

```

**** Places we want to get to easily

```

```

 * Start of the table where we'll store the data as it gets read
 * The table is organized as a set of successive 6 sensor readings
 * It can be placed somewhere else once we know our memory allocation
 * a little better

```

```

TABLSTRT EQU $0003

```

```

*** Overhead for 8-bit stuff

```

```

 * Hardware control register, used to turn on A/D power
OPTION EQU $1039

```

```

 * Control register to both initiate reads and determine what kind to do
ADCTL EQU $1030

```

```

 * Registers where A/D results are deposited after a read

```

```

ADR1 EQU $1031

```

```

DR2 EQU $1032

```

```

ADR3 EQU $1033

```

*** Overhead for 12-bit stuff

* The location where we select which channel to read

ADSLCT EQU \$B5F8

* The location where we write to initiate a conversion

ADSTRT EQU \$B5FA

* The previous is where we will get back our data too!

* Main program *

* Store Y

PSHY

* Turn on 8-bit A/D

LDAA #%10000000

ORAA OPTION * This modifies only ADPU bit

STAA OPTION

* Get ready to use Y for indexed addressing to copy data to table

LDY #TABLSTRT

* Read data from 8-bit A/D's

* Start a sweep of readings through the four input ports

* (#4-#7 in this version because CC and CD are 0 and 1 not 0 0)

BGNRD LDAA #%00010100

STAA ADCTL

* Wait for them to get done

* (We may need to change this to make it spiffier and optimize

* (time stuff)

LDAB #\$FF

DLY1 DECB

BNE DLY1

* METHOD 2 (15 bytes 1/3 the # of cycles)

* Direct copies

LDAA \$1031

STAA \$00

LDAA \$1032

STAA \$01

LDAA \$1033

STAA \$02

* Read data from 12-bit A/D's

* Method 1 (24 bytes, may optimize by switching X and Y)

* Select first channel and set counter

LDAB #05

LDAA #02

* Select channel

CPYPRS STAB ADSLCT

* Initiate conversion

STAB ADSTRT

* Load results into register X

LDX ADSTRT

* Store results in table

STX 0,Y

* Move to next table location

INY

INY

* Select next channel

INCB

* Decrement counter

DECA

* If counter is ≥ 0 keep looping

BGE CPYPRS

* Bring Y back

PULY

* Delay

* This routine just does a decremented Y count that lasts 1 ms for

* however many times are specified in the register A when the routine

* is called.

*DELAY PSHY

* TSTA

* BEQ DERT

*DELOOP LDY #\$00C8

*DEAGAIN BEQ DEAHEAD

* DEY

* BRA DEAGAIN

*DEAHEAD DECA

* BNE DELOOP

*DERT PULY

* RTS

#endasm

```
pokeb(b1+i, peekb(0x0000));  
pokeb(b2+i, peekb(0x0001));  
pokeb(b3+i, peekb(0x0002));  
poke(b4+i, peek(0x0003));  
poke(b5+i, peek(0x0005));  
poke(b6+i, peek(0x0007));  
}
```

```

/* File: READDATA.C
 * Written 8/14/95 by ctillier
 * -----
 * This function uses the ScanAD function to scan three 8-bit and three
 * 12-bit A/D channels. It does so however many times required, and
 * stores the results in the three char arrays t1, t2, t3 and int arrays
 * p1, p2 and p3.
 * -----
 */

```

```

ReadData(t1,t2,t3,p1,p2,p3)
char* t1;
char* t2;
char* t3;
int* p1;
int* p2;
int* p3;
{
    int i;

    for (i = 0; i <= NUMREAD; i++) /* The loop really does go around */
    {
        /* NUMREAD times. This is a bug */
        ScanAD(i,t1,t2,t3,p1,p2,p3); /* in the Small C compiler. */
    }
}

```

```

/* Modified c library code to do a logical shift right four times
 * This should logical shift right the two byte number at 'addr' by
 * 'val' times
 */

```

```

bit_shift(addr,val)
int addr;
char val;
{
    #asm
    * Load in address to be modified
      LDX ARG2,Y
    * Load in # of times to shift
      LDAB ARG1+1,Y
    * Get ready to use Y for something else for just a moment
      PSHY
    * Transfer B to Y so we can count with Y and use D for something else
      XGDY
    * Load in memory double byte to D
      LDD 0,X
    * Logical shift it right
      SHIFT LSRD
    * Decrement Y
      DEY
    * If we're not done yet branch back
      BNE SHIFT
    * Put the modified double byte number back where it came from
      STD 0,X
    * Get back whatever was in Y
      PULY
    #endasm
}

```

```
ProcessData(b1,b2,b3,b4,b5,b6)
```

```
char* b1;
```

```
char* b2;
```

```
char* b3;
```

```
int* b4;
```

```
int* b5;
```

```
int* b6;
```

```
{  
    int i;  
    int totalt1;  
    int totalt2;  
    int totalt3;  
    int finalt;  
    int totalp1;  
    int totalp2;  
    int totalp3;  
    int finalp;
```

```
    totalt1 = 0;
```

```
    totalt2 = 0;
```

```
    totalt3 = 0;
```

```
    for (i = 0; i <= NUMREAD; i++) {
```

```
        totalt1 += peekb(b1 + i);
```

```
        totalt2 += peekb(b2 + i);
```

```
        totalt3 += peekb(b3 + i);
```

```
    }
```

```
    /* TBC: Error checking on the sensors. For now, just an average. */
```

```
    finalt = (totalt1 + totalt2 + totalt3) / (NUMREAD * 3);
```

```
    poke(0x000c, finalt); /* reading ends up in 0x000d */
```

```
    totalp1 = 0;
```

```
    totalp2 = 0;
```

```
    totalp3 = 0;
```

```
    for (i = 0; i <= NUMREAD; i++) {
```

```
        bit_shift(b4 + i, 4);
```

```
        totalp1 += peek(b4 + i);
```

```
        bit_shift(b5 + i, 4);
```

```
        totalp2 += peek(b5 + i);
```

```
        bit_shift(b6 + i, 4);
```

```
        totalp3 += peek(b6 + i);
```

```
    }
```

```
    /* TBC: Error checking on the sensors. For now, just an average. */
```

```
    finalp = ((totalp1 / NUMREAD) + (totalp2 / NUMREAD) + (totalp3 / NUMREAD)) / 3;
```

```
    poke(0x000e, finalp);
```

```
StoreData()
{
    unsigned int memptr;
    memptr = peek(MEM_PTR);

    if (memptr >= ENDSTOR) return;

    poke(memptr, peek(0x000e));
    memptr += 2;
    pokeb(memptr, peekb(0x000d));
    memptr++;
    poke(MEM_PTR, memptr);
}
```

```
/* File: TNC_SEND.C
```

```
* -----  
* This function send the string message to the serial output (which  
* should be configured outside this function). The message is  
* formatted such that a Kantronics KPC-3 terminal node controller  
* (set to "host mode") can understand it. Refer to the Kantronics  
* manual for more information.  
* -----  
*/
```

```
TncSend(message, stream) char message[]; FILE stream;
```

```
{  
    fputc(0xc0, stream);  
    fputc('D', stream);  
    fputc('1', stream);  
    fputc('A', stream);    /* not sure why this needs to be A */  
    fputs(message, stream);  
    fputc(0xc0, stream);  
    fputc(0x0A, stream);  
}
```

```
ReadComm(string)
char* string;
{
    int i;
    char* indx;

    indx = string;
    for (i = 0; i <= MAX_BUFF; i++) {
        *indx = SER_in();
        indx++;
    }

    for(i = 4; i < 7; i++) {
        string[i-4] = string[i];
    }
    string[4] = '\0';
}
```



```
ParseMessage(string)
char* string;
{
    if (string[0] == 's') {
        if (string[1] == 'e') {
            if (string[2] == 'n') {
                if (string[3] == 'd') {
                    return TRUE;
                }
            }
        }
    }
    return FALSE;
}
```

```

/* File: TRANSMIT.C
 * Written 08/17/95, ctillier
 * -----
 * This function takes MAXSAMPLE readings stored in long-term memory and
 * writes them each to a string to be sent out. Instead of a binary data
 * stream (much more compact), we use conversion to hex ascii so that the
 * data can be transferred as text and handled with a plain-vanilla
 * terminal program. This is not unlike UUencoding in spirit.
 * -----
 */

```

```

Transmit(stdout)
FILE stdout;
{
    int i;
    char* msgptr;    /* pointer to walk along message */

    /* Here's what the out message looks like:
     * Position: 1  2  3  4  5  6  7
     * Content:  F  P  P  P  T  T  NULL
     * where F is flags, P is pressure, T is temperature.
     */

```

```

    TncSend("BEGIN DATA\n", stdout);

```

```

    for (i = 0; i <= MAXSAMPLE; i++) {
        msgptr = MESSAGE;
        itoha(peek(BEGINSTOR + 3*i), msgptr);
        msgptr += 4;
        atoha(peekb(BEGINSTOR + 2 + 3*i), msgptr);
        msgptr += 2;
        *msgptr = '\n';
        msgptr++;
        *msgptr = '\0';
        TncSend(MESSAGE, stdout);
    }

```

```

    TncSend("END DATA\n", stdout);
}

```

```
/* Based on the great Jimmy Hendrix's itoa, souped up by Clem Tillier
** itoha(n,s) - Convert n to hexadecimal characters in s
*/
```

```
itoa(n, s) char *s; int n; {
    char *ptr;
    ptr = s;
    do {
        *ptr++ = n % 0x10 + '0';
        if (*(ptr - 1) > ':') *(ptr - 1) += 7;
    } while ((n = n / 0x10) > 0);

    /* pad rest with zeros */

    while (ptr < s + 3) {
        *ptr++ = '0';
    }

    *ptr = '\0';
    reverse(s);
    return (s);
}
```

```
atoha(c, s) char *s; char c; {  
    char *ptr;  
    ptr = s;  
    *ptr = c % 16 + '0';  
    if (*ptr > ':') *ptr += 7;  
    ptr++;  
    *ptr = (c / 16) % 16 + '0';  
    if (*ptr > ':') *ptr += 7;  
    ptr++;  
    *ptr = '\0';  
    reverse(s);  
    return(s);  
}
```

```
/* written by M. Taylor */  
strlen(s) char *s; {  
    int i;  
    i=0;  
    while (*s++) i++;  
    return i;  
}
```

/* Taken from J.E. Hendrix' Small C Compiler V2.2 */

```
reverse(s) char *s; {  
    char *j;  
    int c;  
    j = s + strlen(s) - 1;  
    while(s < j) {  
        c = *s;  
        *s++ = *j;  
        *j-- = c;  
    }  
}
```

Increment()

```
{  
    int sample;  
  
    sample = peek(SAMP_ADDR);  
    sample++;  
    poke(SAMP_ADDR, sample);  
}
```

FlushData()

```
{  
    int sample;  
    int i;  
  
    /* decrement the sample counter by MAXSAMPLE */  
  
    sample = peek(SAMP_ADDR);  
    sample -= MAXSAMPLE;  
    poke(SAMP_ADDR, sample);  
  
    /* move all remaining samples in memory down to the beginning  
     * of the data storage */  
  
    for (i = 0; i <= sample; i++) {  
        poke(BEGINSTOR + 3*i, peek(BEGINSTOR + (MAXSAMPLE + i)*3));  
        pokeb(BEGINSTOR + 3*i + 2, peekb(BEGINSTOR + (MAXSAMPLE + i)*3 + 2));  
    }  
}
```



```

RTSon()
{
#asm
    Establish where the addresses are
    * Pin direction control address for Port D
    * DDRD EQU $09
    * Pin value address for Port D
    * PORTD EQU $08
    * Pin #03 being used for RTS
    * RTSMASK EQU $20

    * Set DDRD correct and turn on RTS pin
        LDX #$1000
        FCB $1C,$09,$20
        FCB $1C,$08,$20
    * FCB DDRD
    * FCB RTSMASK
    * FCB $1C
    * FCB PORTD
    * FCB RTSMASK

    * BSET DDRD,RTSMASK
    * BCLR PORTD,RTSMASK

#endasm
}

```

```

RTSoff()
{
#asm
* Establish where the addresses are
* Pin direction control address for Port D
* DDRD EQU $1009
* Pin value address for Port D
* PORTD EQU $1008
* Pin #03 being used for RTS
* RTSMASK EQU $20

* Start program

* Set DDRD correct and turn on RTS pin
* Method 3
* LDAA #$20
* ORAA $1009
* EORA $1008

* Method 2
    LDX #$1000
    FCB $1C,$09,$20
    FCB $1D,$08,$20
* Method 1
* FCB DDRD
* FCB RTSMASK
* FCB $1C
* FCB PORTD
* FCB RTSMASK

* BSET DDRD,RTSMASK
* BCLR PORTD,RTSMASK

#endasm
}

```

OpenEars(stdout)

FILE stdout;

{

int sample;

sample = peek(SAMP_ADDR);

fputs("Checking to see if Maxsample exceeded\n", stdout);

if (sample > MAXSAMPLE || sample == MAXSAMPLE) {

fputs("Maxsample exceeded, turning on IRQ\n", stdout);

#asm

CLI

#endasm

}

}

Appendix IV

LiSOC12 Battery Test Report

Micro-Met Research Project Memorandum

Subject: LiSOCl₂ Battery Test Report
By: Steve Merrihew
Date: 5/20/96

CONTENTS:

Introduction	Page 1
Test Facilities	Page 1
Test Requirements	Page 2
Test Plan	Page 2
Test Report	Page 4
Figures	Page 12

INTRODUCTION:

In the Winter of 1995 a series of battery tests were performed to provide an initial characterization of Tadiran model TL-2300 LiSOCl₂ (Lithium Thionyl Chloride), D-cell batteries within the estimated temperature extremes and power profile for the Micro-Met mission. These tests were defined by Steve Merrihew and performed by Lynn Hofland in the battery test lab located in building 244, NASA/Ames. This battery test coincided with the NASA/Ames - Stanford JRI project to design, assemble and test the electronic components for a prototype Micro-Met surface station.

The general characteristics of the LiSOCl₂ cell is long life with very good energy density at low current operation and reasonable temperatures. The Micro-Met thermal control system is designed to provide an internal environment of -40 °C to +40 °C, therefore, the operational characteristics of the LiSOCl₂ cells within this temperature range are critical to the success of the design. Copies of the pertinent product literature describing the Tadiran LiSOCl₂ cell chemistry and operational characteristics are attached at the end of this report. Please note that the TL-2300 D-cell batteries tested do not have the short circuit protection provided by the polyswitch (a positive temperature coefficient resistor) described in the attached Tadiran materials.

TEST FACILITIES:

NASA/Ames has several temperature controlled test chambers suitable for these tests. Perhaps more importantly, the Galileo LiSO₂ (Lithium Sulfur Dioxide) battery test program was conducted in building 244. Facilities available for the tests include:

- Thermal test chambers, providing at least -40 °C to +40 °C
- Battery support racks and instrumentation for up to five D-cell batteries
- Measurement of cell voltage, impedance and complex impedance
- Thermocouple instrumentation to measure cell temperature
- Ability to simulate varied circuit loads (at constant current or resistance)

TEST REQUIREMENTS:

The NASA/Ames, Stanford University team provided the following:

- Test plan
- Tadiran LiSOCl₂ D-cell batteries (model TL-2300) and manufacturer's documentation (up to six batteries are available)
- Baseline Power profile (assuming a 3.45 Volt battery, constant resistance)
 - communication event power = approx. 3.9 W for approx. 10 seconds (test at a constant 3.05 Ohms)
 - data collection event power = 0.9 W for approx. 10 seconds (test at a constant 13.23 Ohms)
 - steady state power = approx. 6 mW for approx. 30 seconds (test at a constant 1983.75 Ohms)
- Temperature set points
 - Tests are to be performed at +40, +20, 0, -20, -30, -40, -50 °C
 - A cold case is to be performed by chilling the cells to approx. -80 °C
 - A hot case is to be performed by heating the cells to approx. +60 °C
 - Approximately 4 hours will be required for the battery cell internal temperature to equalize with the test chamber temperature at each temperature set point.

The NASA/Ames test facilities will provide the following:

- Thermal test chamber with approximately -80 °C to +60 °C capability
- Battery support racks and test instrumentation leads
- Test circuit simulator (constant resistance loads)
- Time indexed measurements of:
 - Cell voltage
 - Cell temperature
 - Cell impedance

TEST PLAN:

The baseline power requirement test sequence (after holding at each temperature set point for four hours) is as noted below, note that all resistances are calculated for a single cell voltage of 3.45 V:

- steady state power for 30 sec. (6 mW)
(constant resistance load = 1983.75 Ohms)
- data collection power for 10 sec. (0.9 W)
(constant resistance load = 13.23 Ohms)
- steady state power for 30 sec. (6 mW)
(constant resistance load = 1983.75 Ohms)
- data collection power for 10 sec. (0.9 W)
(constant resistance load = 13.23 Ohms)
- steady state power for 30 sec. (6 mW)
(constant resistance load = 1983.75 Ohms)
- communication power for 10 sec. (3.9 W)
(constant resistance load = 3.05 Ohms)

- steady state power for 30 sec. (6 mW)
(constant resistance load = 1983.75 Ohms)

Each battery cell test is to include measurements of the following:

Battery cell voltage (at approx. 10 Hz)

Battery cell temperature (at approx. 10 Hz)

Battery cell impedance (internal resistance) (at approx. 10 Hz)

- 1) The battery cell(s) are to be tested at the following resistance (hence power) settings for each of the temperature set points, allow approximately 2 minutes between power setting tests (tests (a) through (c)):
 - a) baseline (as defined in Test Requirements and above)
 - b) 2 times baseline
 - c) 0.5 times baseline
- 2) Each resistance setting is to be tested at each of the following operational temperature set points (in this order, with 4 hours hold time at each temperature):
 - 0, -20, -30, -40, -50, +20, +40 °C
- 3) A cold case is to be run as follows:
 - Chill to -65 °C, hold for 4 hours; measure cell temperature, voltage and internal resistance
 - Warm to 0 °C, hold for 4 hours
 - Test at 0 °C; run through baseline, 2*baseline and 0.5*baseline
- 4) A hot case is to be run as follows:
 - Warm to +60 °C, hold for 4 hours; measure cell temperature, voltage and internal resistance
 - Cool to 0 °C, hold for 4 hours
 - Test at 0 °C; run through baseline, 2*baseline and 0.5*baseline

The test therefore consists of:

- 7 baseline temperature set points
- 2 extreme temperature tests
- 9 power profiles per temperature set point
(communication, data collection and steady state power at 0.5, 1.0 and 2.0 times the baseline Micro-Met power requirements)
- 3 measurements at approx. 10 Hz for each test
(cell voltage, cell temperature, cell impedance)

TEST REPORT:

*Important Note: The power profiles defined in the Test Plan are in error. The baseline Micro-Met battery assembly is six D-cells connected in parallel. In this configuration the total battery voltage is equal to that of a single cell and the total battery current equals six times a single cell current. The baseline power profile defined in the Test Plan failed to take this into account when testing a single cell, hence the baseline power profile current requirements are six times too high. Therefore, the tests at 2 times the baseline exceed the actual design requirements by 12 times, and the tests at 0.5 times the baseline exceed the actual design requirements by 3 times. The net result is that the baseline and 2*baseline requirements are unreasonably high and should not be interpreted as real requirements for a Micro-Met mission. The tests conducted at 0.5 times the baseline requirement are reasonable however and represent a worst case of 3 times the design requirement.*

TEST RESULTS:

General notes: The tests are conducted at constant resistance loads to better model actual operation. The actual cell current is therefore a function of instantaneous cell voltage divided by the resistance load. The most important test result is the ability of the LiSOC12 cell to provide adequate voltage during the tests. The cutoff voltage is defined in this analysis as 75% of the baseline cell voltage (hence cutoff = 2.6V). The data files are defined in the following Table.

Table 1: Test Run Summary

Test Run	Test Condition	Test Date	Notes
A	0 °C	12/1/95	first use of cell
B	0 °C	12/1	repeat of "A"
C	0 °C	12/4	repeat of "A"
D	-20 °C	12/4	
E	-30 °C	12/5	
F	-40 °C	12/5	
G	-50 °C	12/5	
H	0 °C	12/6	
I	+20 °C	12/6	
J	+40 °C	12/7	
K	0 °C	12/8	
L	-65 °C	12/8	no power tests run
M	0 °C	12/8	post cold case test
N	+20 °C	12/11	
O	+60 °C	12/12	no power tests run
P	0 °C	12/12	post hot case test

Run "A" (0 °C):

A principle characteristic of any LiSOC12 cell is the formation of a "passivation layer" on the internal cell electrodes. This passivation layer is a resistive layer formed from long periods of non-use. Passivation layer formation is accelerated by storage at high temperatures. While this internal resistance improves the shelf life of the LiSOC12 cell, it presents a problem upon first use of the cell. Until the passivation layer is broken down ("burnt off") by a high current load the cell cannot provide adequate voltage at low currents. The effect of this passivation layer is evident in the plots of cell current, voltage and resistance versus time (Figures A1 to A3).

Figure A1 presents the current (amps) performance of the cell for baseline (at time equals approximately 0 to 2 minutes), 2 times baseline (3 to 5 minutes) and 0.5 times baseline (5 to 8 minutes) estimated power requirements (see the Test Plan for details). As is apparent from the first communications event (at time = 2 minutes), the cell is not able to provide the desired current of 1130 mAmps. For this same test (baseline communications), the voltage (Figure A2) falls to approximately 0.7 Volts. As is apparent from Figure A3, the cell resistance initially peaks at approximately 80 Ohms, dropping to approximately 5 to 7 Ohms after the first baseline communication event (at time = 2 minutes). The resistance continues to drop after each of the large current events (data collection and communication), eventually reaching approximately 2 to 3 Ohms. With the passivation layer present, this battery therefore is not able to provide adequate power for a 0.5*baseline communication event.

The third set of tests (the 0.5 times baseline) shows the dramatic improvement of the cell performance as the passivation layer begins to burn off and the power requirements drop. The cell voltage (Figure A2) never drops below approximately 2.4 Volts (approximately 70% of the baseline open circuit voltage) at time = 7 minutes.

Cell temperature is plotted in Figure A4. Note that there is slight cell warming for each run, but the effect is essentially negligible.

Run "B" (0 °C):

Run B, a repeat of Run A, demonstrates the improved performance of the cell as the passivation layer continues to dissipate. Figure B3 plots the cell resistance versus time, with a peak resistance of approximately 8 Ohms dropping to approximately 2 Ohms after the first baseline level data collection event. The cell current and voltage performance is therefore improved somewhat (Figures B2 and B3), however the cell voltage (at 0.5 times baseline communications, time = 7 minutes) again falls to approximately 70% of the baseline open circuit voltage. Figures B5 and B6 plot the recovery of the cell after the power tests. It can be seen that the cell voltage recovers to the full value of approximately 3.55 Volts while the resistance recovers to approximately 2 Ohms. Figure B7 plots the time history of the cell temperature. The variation in the test chamber temperature (approximately 0.9 °C to -0.8 °C) dominates the internal cell heating effects (high frequency data plotted from 0 to 7 minutes).

Run "C" (0 °C):

Run C, again a repeat of Run A, demonstrates the continued decrease in internal cell resistance as the passivation layer is burnt off. The resistance data plotted in Figure C3 is seen to level off at approximately 1 Ohm, some 80 times less than the peak initial cell resistance tests in Run A. The effect of this reduced internal resistance is apparent in the current and voltage plots (Figures C1 and C2). These plots are found to be less "peaky" than those of runs A and B, indicating that the cell performance is more steady at high power loads. For the first time, the 0.5 times baseline communication cell voltage, 2.5 Volts, exceeds the 75% cutoff limit. Therefore, the cell is now able to provide adequate power for a 0.5* baseline communication event

Table 2 summarizes the performance improvements due to the loss of the passivation layer. Note that the voltage data is for the 0.5*baseline communications event (at approximately 7 minutes into each test run).

Table 2: Effects of Passivation Layer Burn-Off

Test Run	Initial Internal Resistance - Peak (Ohms)	Final Internal Resistance (Ohms)	Communication Event voltage (Volts)
A	80	2	2.35
B	9	1.8	2.35
C	6	1.1	2.5

The principle conclusion to draw from runs A, B and C is that the passivation layer must be dissipated before the cell is to be used for basic operations. Therefore, a high current load is required at the beginning of the Micro-Met mission surface operations.

Run "D" (-20 °C):

The performance of the LiSOCl₂ cell is reduced in cold conditions. Comparing Figures D1 and D2 with Figures C1 and C2 demonstrates the overall loss of performance (current and voltage) as the temperature drops to -20 °C. The voltage drops below the defined cutoff (to approximately 2.35) Volts for the 0.5* baseline communication event (at time = 7 minutes). Internal resistance (Figure D3) remains at approximately 1.5 Ohms.

Runs "E", "F" and "G" (-30 °C, -40 °C and -50 °C):

As with run D, decreasing temperature reduces the performance (current and voltage) of the LiSOCl₂ cell. Along with the reduced current and voltage performance, the internal cell resistance is found to increase slightly. The cell maximum voltage was also found to decrease with decreasing temperature. These results are summarized in Table 3.

Table 3: Summary of Cold Case Results

Run	Maximum Cell voltage (Volts)	Communication Event voltage (Volts)	Final Internal Resistance (Ohms)
D (-20 °C)	3.48	2.35	1.7
E (-30 °C)	3.35	2.25	1.85
F (-40 °C)	3.30	2.10	2.75
G (-50 °C)	3.25	1.85	4.3

As listed in the table, the performance of the cell for the 0.5*baseline communication event at -50 °C drops below 2.0 Volts, to only 54% of the baseline cell voltage (assumed to be 3.45 Volts). The performance at -40 °C (2.1 Volts, or 61%), while below the cutoff voltage defined earlier, may represent the lowest feasible operating temperature for the LiSOC12 cell.

Run "H" (0 °C):

Following the cold operations cases (Runs D through G), a test was performed at 0 °C to investigate whether the cell exhibited any lasting effects after the cold temperature operation. The current and voltage performance is good for the 0.5* baseline case (Figures H1, H2). The minimum voltage for the communications event was found to meet the cutoff of 2.6 Volts, or 75% of the baseline cell voltage. The maximum cell voltage (3.58 V) is approximately equal to the 0 °C results from Run C and represents an increase from the -50 °C case (3.25 V). The internal cell resistance of approximately 0.9 Ohms shows the continued effects of passivation layer burn-off when compared to Run C, and is significantly less than the 4.3 Ohms for Run G (-50 °C). These results indicate that the LiSOC12 cell has recovered completely from the cold operations.

Run "I" (+20 °C):

The results from +20 °C indicate a general improvement in cell performance compared to the 0 °C cases. The current (Figure I1) and voltage (Figure I2) characteristics are reasonably flat, with a minimum voltage of 2.8 Volts for the 0.5*baseline communications event (81% of the baseline cell voltage). The internal cell resistance (Figure I3) remains low, with a steady value of approximately 650 mOhms. Figures I5 and I6 depict the long term characteristics of the cell voltage and resistance respectively. The voltage is found to recover completely to approximately 3.6 Volts while the cell internal resistance settles at approximately 750 mOhms.

Run "J" (+40 °C):

Continuing the trends from Run I, increasing the cell temperature to +40 °C results in increased cell performance. The minimum cell voltage for the 0.5*baseline communications event is found to be 2.95 Volts (Figure J2) while the internal cell resistance drops to approximately 550 mOhms. The conclusion is that the LiSOC12 cell meets all requirements for operation at +20 °C and +40 °C. Table 4 summarizes the hot case operation results.

Table 4: Summary of Hot Case Results

Run	Maximum Cell voltage (Volts)	Communication Event voltage (Volts)	Final Internal Resistance (Ohms)
I (+20 °C)	3.61	2.79	0.65
J (+40 °C)	3.65	2.95	0.55

Run "K" (0 °C):

Following the hot operations cases (Runs I and J), a test was performed at 0 °C to investigate whether the cell exhibited any lasting effects after the hot temperature operation. The current and voltage performance is good for the 0.5* baseline case (Figures K1, K2). The minimum voltage for the communications event was found to meet the cutoff of 2.6 Volts, or 75% of the baseline cell voltage. The maximum cell voltage (3.58 V) is approximately equal to the 0 °C results from Run C and Run H and represents an decrease from the +40 °C case (3.65 V). The internal cell resistance of approximately 0.75 Ohms is slightly more than the 0.55 Ohms for Run J (+40 °C). These results indicate that the LiSOC12 cell has recovered from the hot operations.

Run "L" (-65 °C, Cold Extreme Case):

Given the extreme temperatures on Mars, the operation of the LiSOC12 cell after exposure to extreme hot and cold temperatures is critical to mission success. The Micro-Met surface operations scenario is to shut down the station during these temperature extremes, therefore placing the station into a housekeeping mode until the temperature falls within ± 40 °C. These extreme temperature exposure tests differ from the hot and cold case tests described above in that the batteries are not operated at the extreme temperature. The tests measured the following (with a current of approximately 380 micro-Amps); the voltage, internal cell resistance and cell temperature. The principle finding from this test is that the voltage (Figure L2) decreases steadily from an initial value of 3.55 Volts to a final measured value of approximately 3.3 Volts. Note that the voltage did not level off, so the expectation is that the voltage would continue to fall, eventually stabilizing at some unknown level. The internal cell resistance (Figure L3) reaches a steady value of 2.6 Ohms from an initial value of 0.8 Ohms. These results, the decrease in open circuit voltage and increase in internal resistance, are similar to that experienced in the cold case operations (runs D through G).

Run "M" (0 °C, Post-Cold Extreme Case):

Following the extreme cold test, the operational characteristics of the cell at 0 °C were tested to determine if there were any lasting effects from the cold temperature exposure. The 0.5*baseline communications event (at time = 7 minutes) plotted in Figure M2 results in a minimum voltage of 2.62 Volts (76% of baseline). The internal cell resistance plotted in Figure M3 holds steady at approximately 0.7 Ohms. The voltage and resistance values are approximately the same as those from runs H and K, indicating that the battery has fully recovered from the exposure to -65 °C (Run L).

Run "N" (+20 °C):

Run N provides an intermediate temperature (+20 °C) run prior to the hot case (Run O). The results from this run are consistent with the first +20 °C case (Run I), with slightly lower internal resistances (Figure N3) (approximately 650 mOhms versus 750 mOhms) and an attendant slight increase in the 0.5*baseline communications event voltage (2.8 Volts versus 2.78 Volts, Figure N2).

Run "O" (+60 °C, Hot Extreme Case):

The hot temperature extreme case was conducted from approximately room temperature, heated to +60 °C for four hours and then cooled to 0 °C. As expected, the cell voltage increased with temperature (Figure O1), reaching a plateau of 3.66 Volts. The internal resistance (Figure O2) is found to first decrease from approximately 0.6 Ohms to 0.5 Ohms, then increase to 1.6 Ohms in this same period of time. The voltage and characteristics are similar to those from Runs I and J (+20 °C and +40 °C respectively). While the initial decrease in internal resistance is similar to Runs I and J, the ultimate increase in internal resistance is a new result. This increased internal resistance indicates that the +60 °C exposure is beginning to create a passivation layer on the cell electrodes.

An interesting feature of Figures O1 (voltage) and O2 (cell internal resistance) is the spike in voltage (to 3.7 Volts) that occurs immediately upon decrease in cell temperature (Figure O3). The internal resistance is seen to lag the voltage, but once the internal resistance reaches a peak of 7 Ohms, the voltage drops, ultimately reaching a value of approximately 3.6 Volts.

Run "P" (0 °C, Post-Hot Extreme Case):

Following the extreme hot test, the operational characteristics of the cell at 0 °C were tested to determine if there were any lasting effects from the hot temperature exposure. A comparison of the current (in Amps) plots for post-hot (Figure P1) and post-cold cases (Figure M1) indicates that the cell performance has been degraded by the exposure to high temperatures (lower currents and more "peaky" plots). The voltage for the 0.5*baseline communications event (at time = 7 minutes) plotted in Figure P2 displays a minimum voltage of approximately 2.5 Volts (72% of baseline) which when compared to Figure M2 indicates a loss of performance from the hot temperature exposure. A comparison of the internal cell resistance plots (Figures P3 and M3) provides the reason for this loss in performance. The high temperature exposure from Run O has apparently created a passivation layer (evident on Figure P3) with an initial resistance of approximately 4.2 Ohms, dropping to 1.0 Ohms by the end of the power cycles. The internal resistance values plotted in Figure M3 (post-cold test) holds steady at approximately 0.7 Ohms. The high temperature has apparently created not only a passivation layer that is burnt off during operations, but a permanent increase in cell internal resistance, indicating that the battery has NOT fully recovered from the exposure to +60 °C (Run O). Note that as this was the final test sequence, it is not known if the cell would recover to approximately 0.7 Ohms of internal resistance as with Run M (immediately prior to the hot extreme case).

TEST CONCLUSIONS:

A brief summary of the voltage performance of the Tadiran TL-2300 D-cell LiSOCl₂ battery is provided in Table 5. Recall that the power profiles were not run for the extreme temperature cases (Runs L and O). The Communications event voltage data is for a 0.5*baseline communications power profile (1.95 W). Note that this represents three times the actual power requirement for the Micro-Met Station operations as described in the note at the beginning of this test report.

Table 5: Voltage Performance Summary

File	Temp. (°C)	Communications Event Voltage (Volts)	Percentage of Baseline Cell Voltage (3.45 V) (%)
A	0	2.35	68
B	0	2.35	68
C	0	2.50	72
D	-20	2.35	68
E	-30	2.25	65
F	-40	2.10	61
G	-50	1.85	54
H	0	2.60	75
I	+20	2.79	81
J	+40	2.95	86
K	0	2.60	75
L	-65	n/a	n/a
M	0	2.62	76
N	+20	2.80	81
O	+60	n/a	n/a
P	0	2.50	72

The conclusions that can be drawn from this testing are as follows:

- 1) **Effect of Passivation Layer Burn-Off:** The cell was not able to provide the required voltages in Runs A and B, and just barely in Run C due to the high levels of internal resistance from the passivation layer. The internal resistance was found to drop dramatically following large current loads. Operational scenarios must include a series of high current loads at the mission start in order to completely remove this passivation layer.

- 2) Voltage Drop off During Cold Temperature Operations: The operation of the cell at cold temperatures (Runs D through G) result in decreasing operational voltages. The practical limit of operation may be -40°C where the cell provides 2.10 Volts (61%). At -50°C the cell can only provide 1.85 Volts (54%) of the normal open circuit voltage. It is therefore critical that the Micro-Met thermal control system provide an operating environment above -40°C .
- 3) Voltage Satisfactory During Hot Temperature Operations: The operational voltage during the hot temperature operations (Runs I and J) each produce satisfactory results and present no operational limitations for the Micro-Met Station.
- 4) Good Recovery from Extreme Cold: The exposure to extreme cold (Run L) resulted in decreasing open circuit voltages. Subsequent operational tests at 0°C (Run M) demonstrated that the cell had completely recovered from the exposure to extreme cold.
- 5) Incomplete Recovery from Extreme Heat: The exposure to extreme high temperatures (Run O) resulted in an increase in internal resistance from the development of a new passivation layer. This passivation layer was not completely "burnt-off" by the subsequent operations at 0°C (Run P). As no further tests were conducted, it is not known if this increase in internal resistance is permanent.

COMMENDATIONS FOR FURTHER TESTING

Subsequent tests of the LiSOC12 batteries for the Micro-Met mission should incorporate the following:

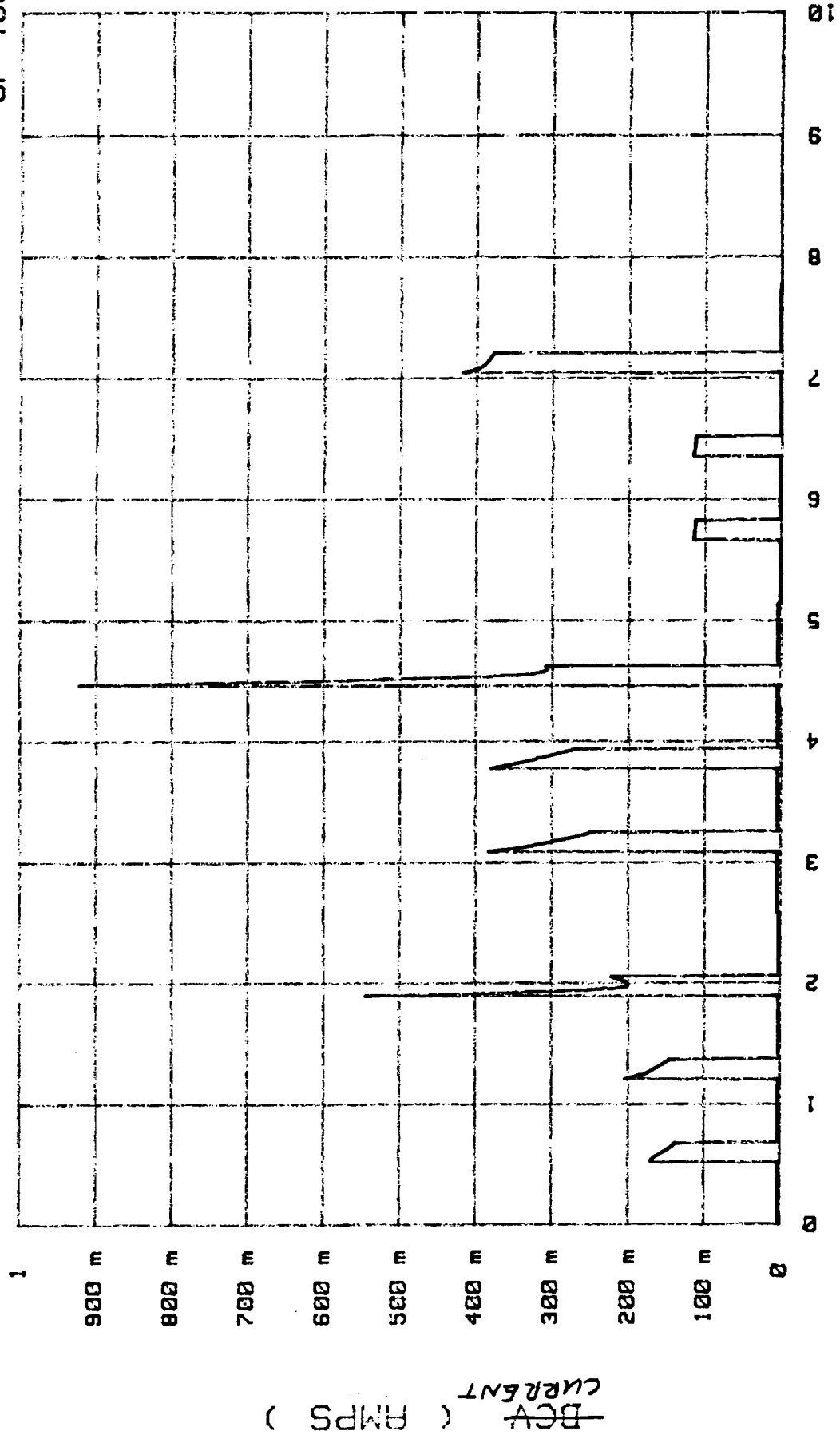
- A correct power profile (see the note at the beginning of the test report)
- Testing of multiple independent cells to determine repeatability
- Further testing at temperature extremes (hot and cold) to determine lifetime effects
- Testing of an integrated battery (several cells)

FIG. A1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409



TIME (MINUTES)

FIG A2

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

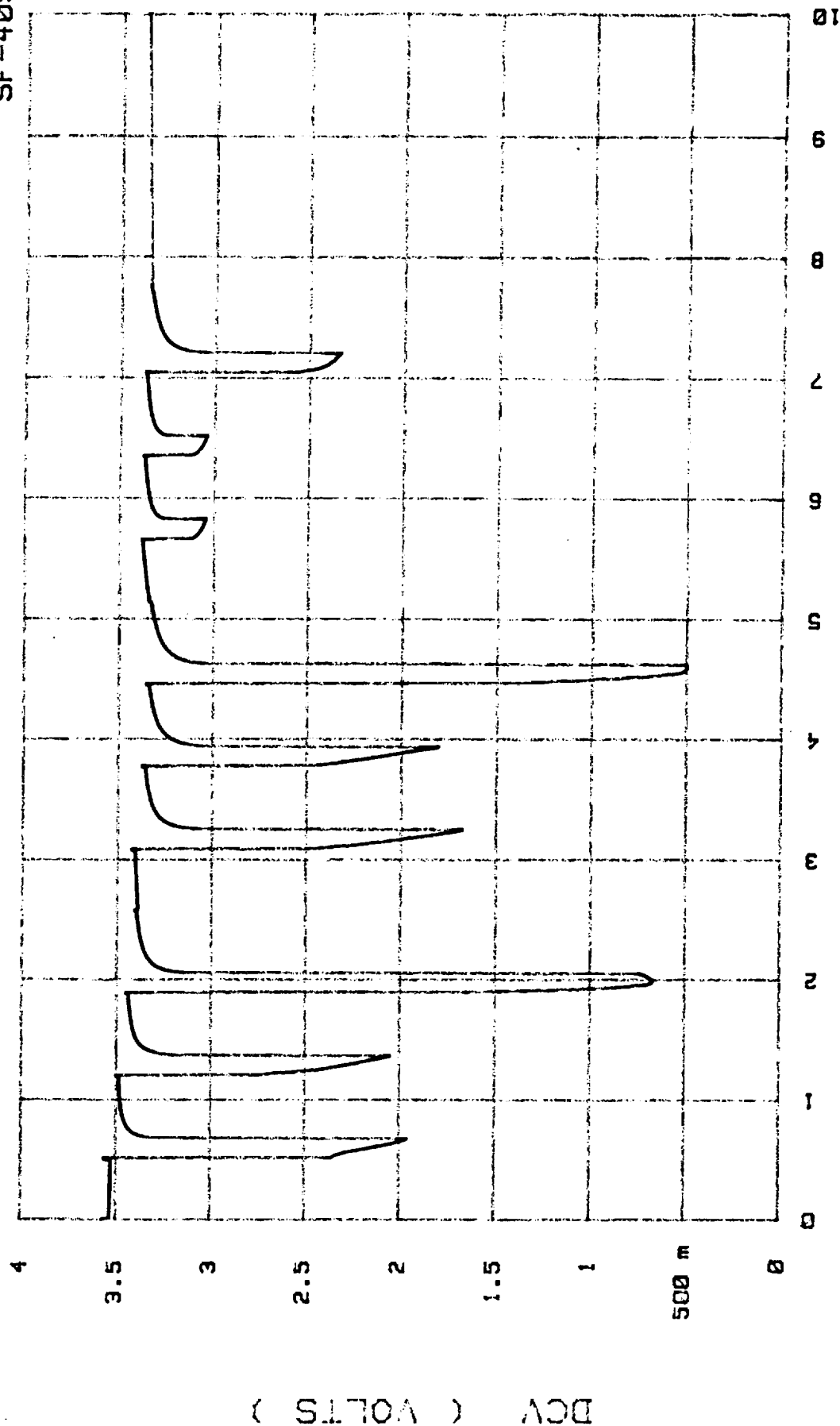
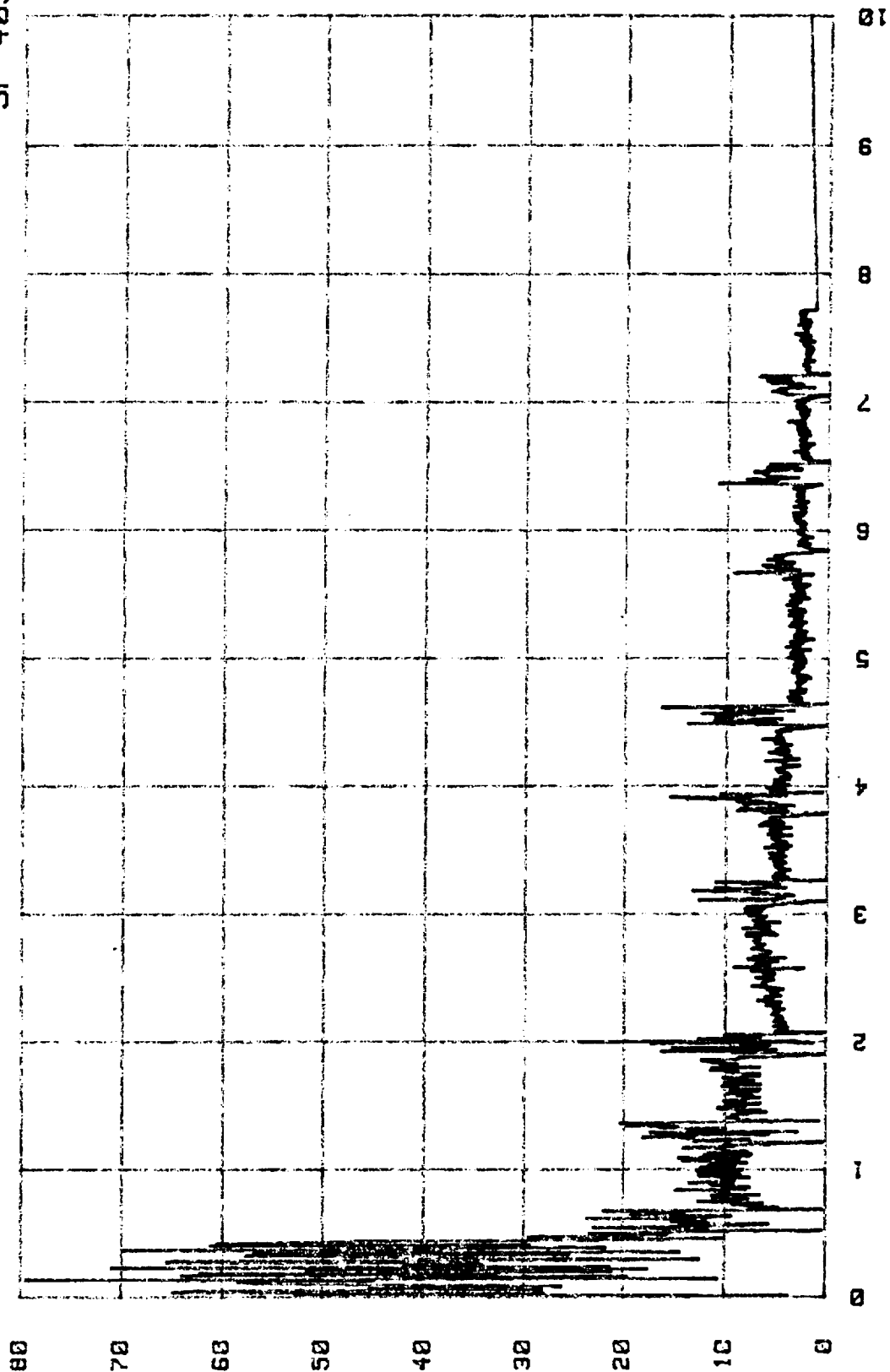


FIG. A3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409



DCV (OHMS)
Resistance

TIME (MINUTES)

FIG. A4

Li/SOC12 CELL PREFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

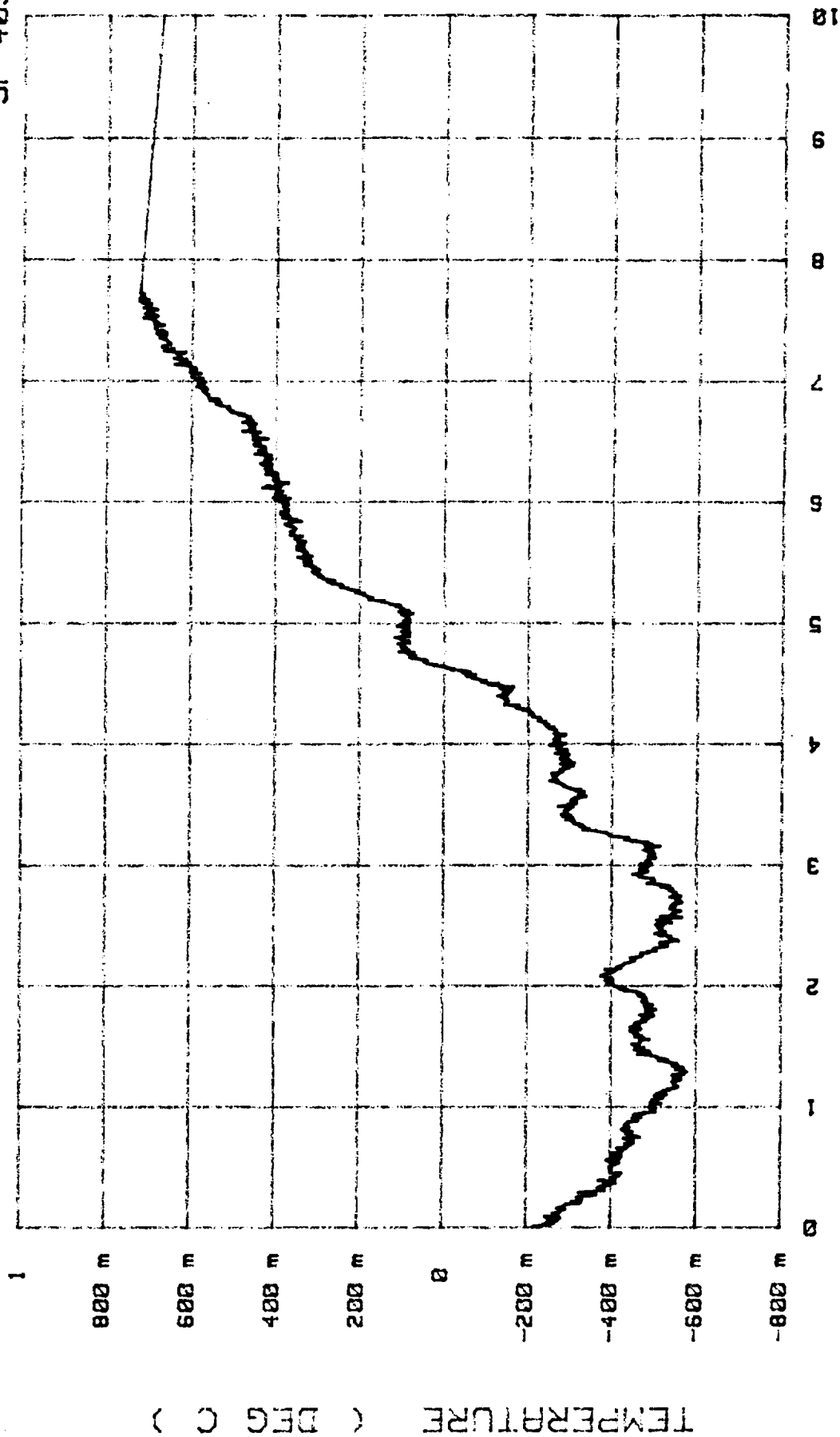


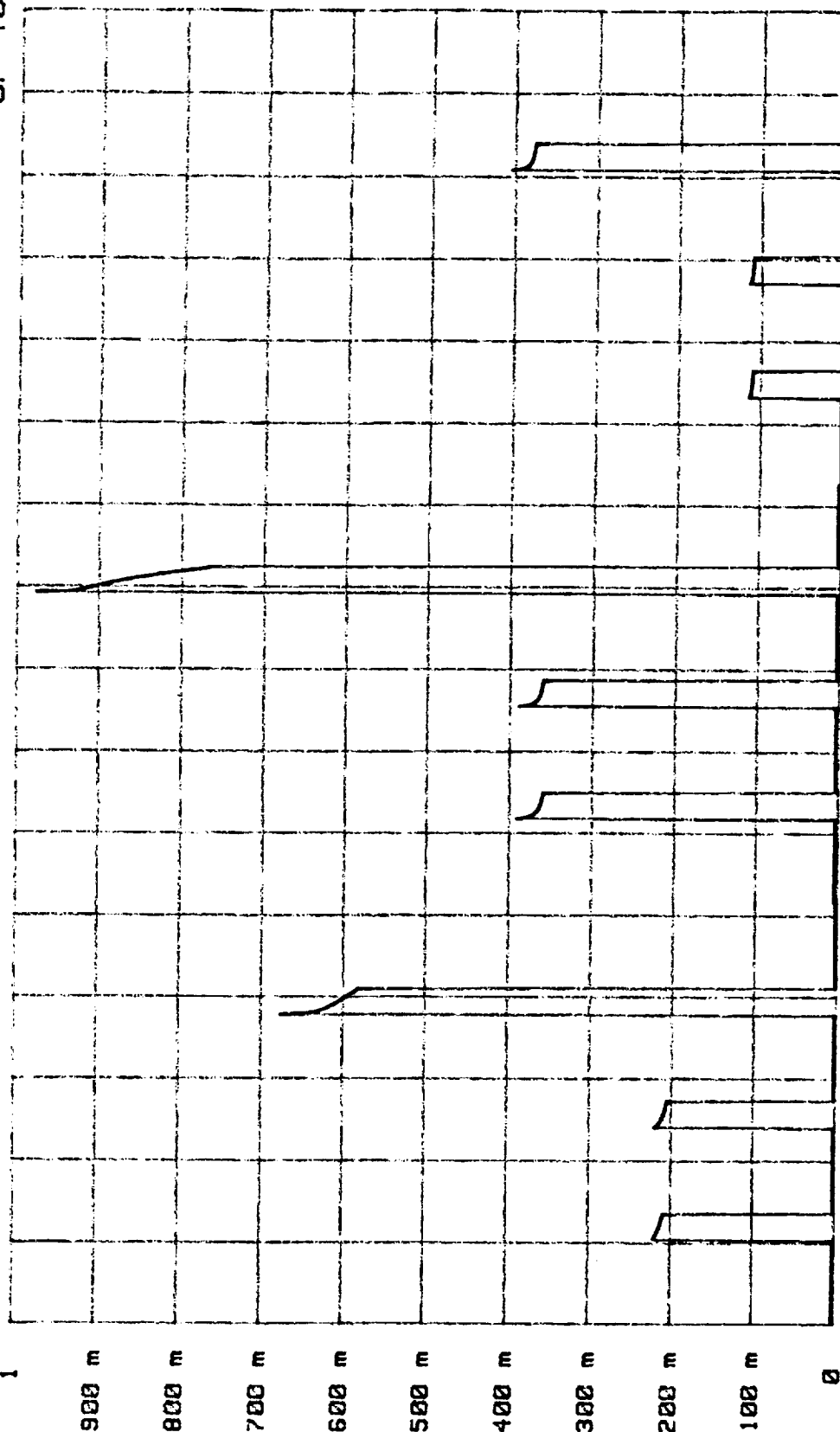
FIG. B1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

CELL #1, SECOND ZERO DEG C TEST.



500 m

TIME (MINUTES)

CELL1_DCH_B: Channel 1

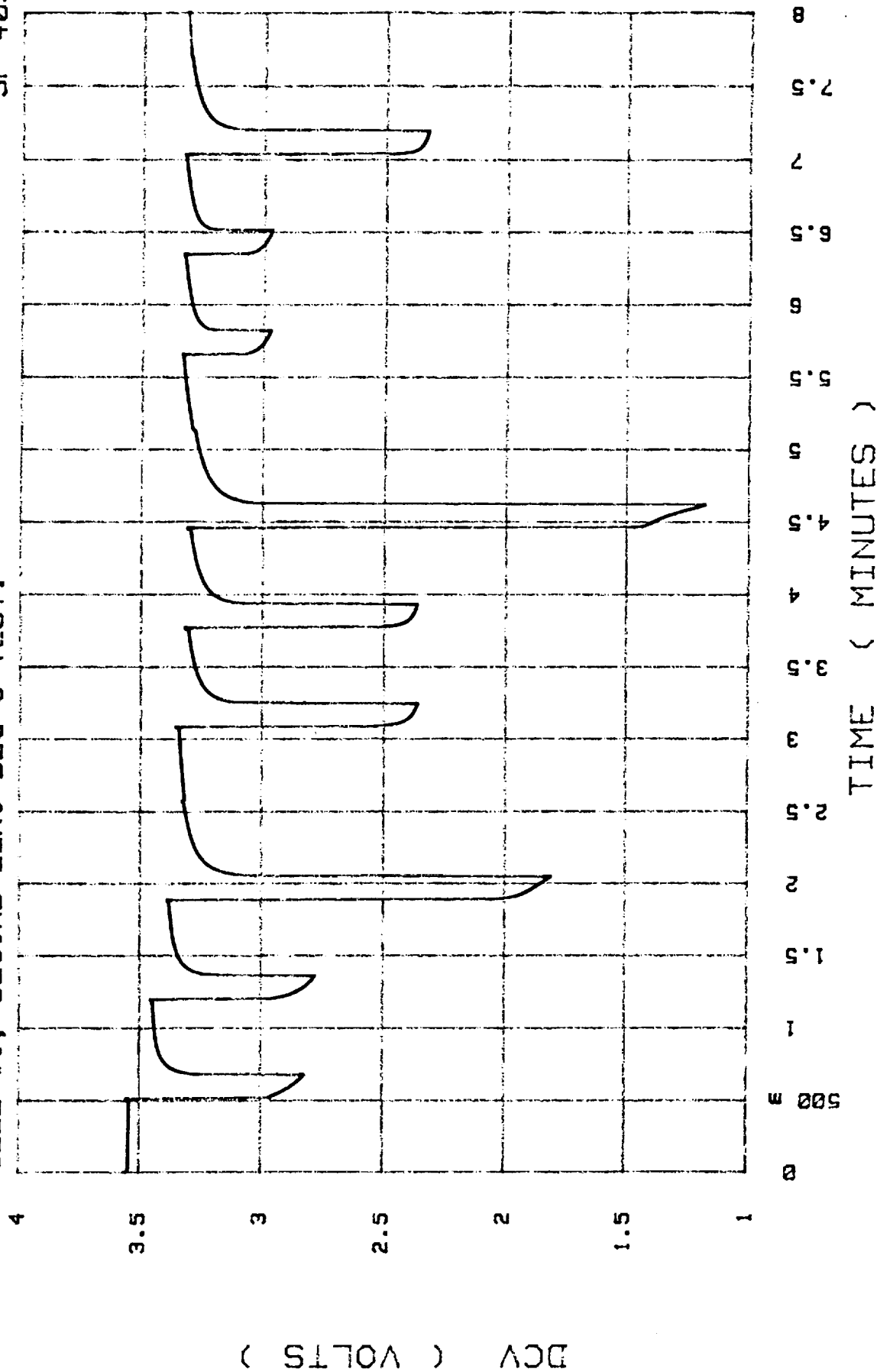
FIG. B2

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

CELL #1, SECOND ZERO DEG C TEST.



CELL1_DCH B: Channel 2

FIG. B3

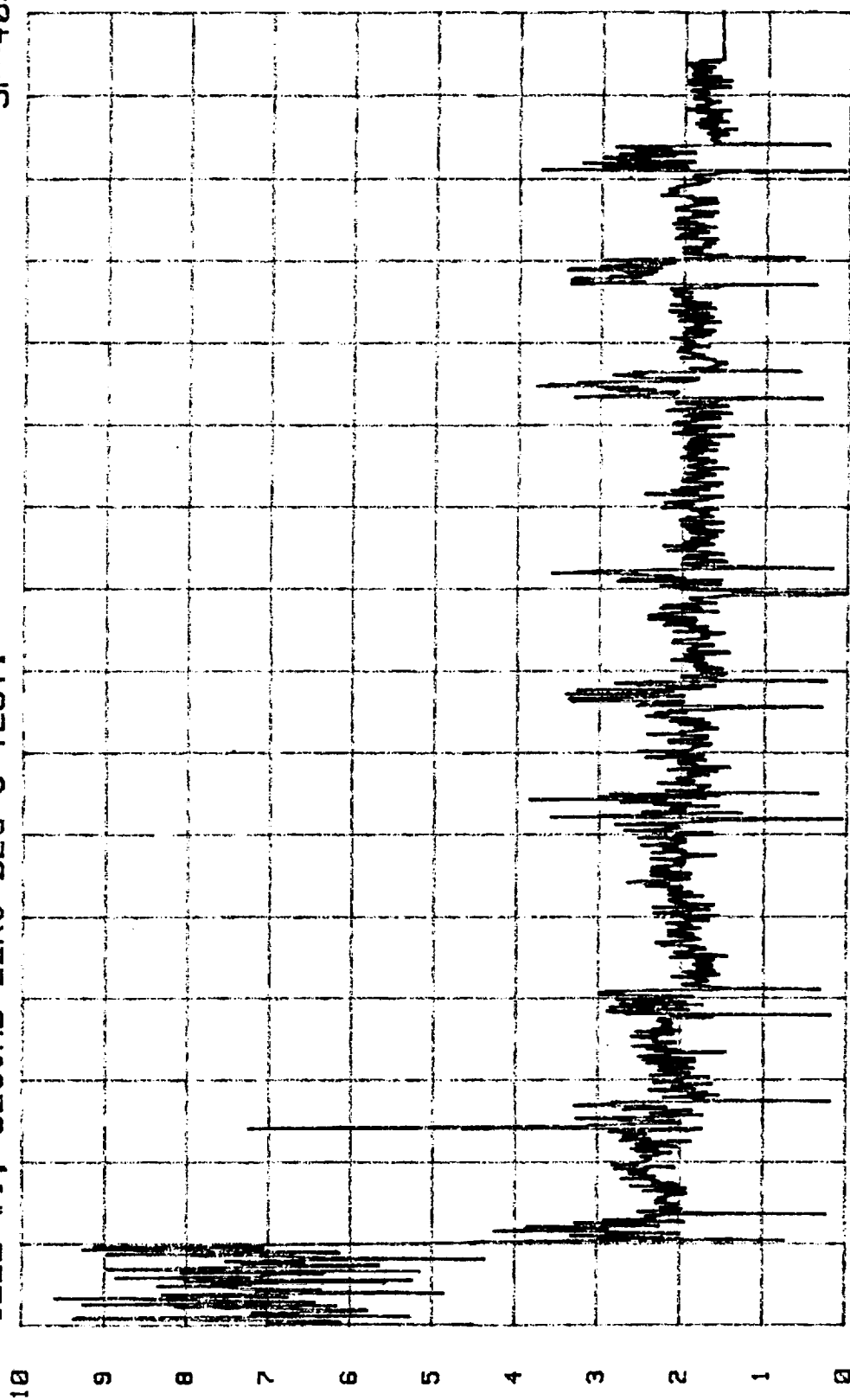
Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995

SF-409

CELL #1, SECOND ZERO DEG C TEST.



500 E

TIME (MINUTES)

CELL1_DCH_B: Channel 3

FIG. B4

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

CELL #1, SECOND ZERO DEG C TEST.

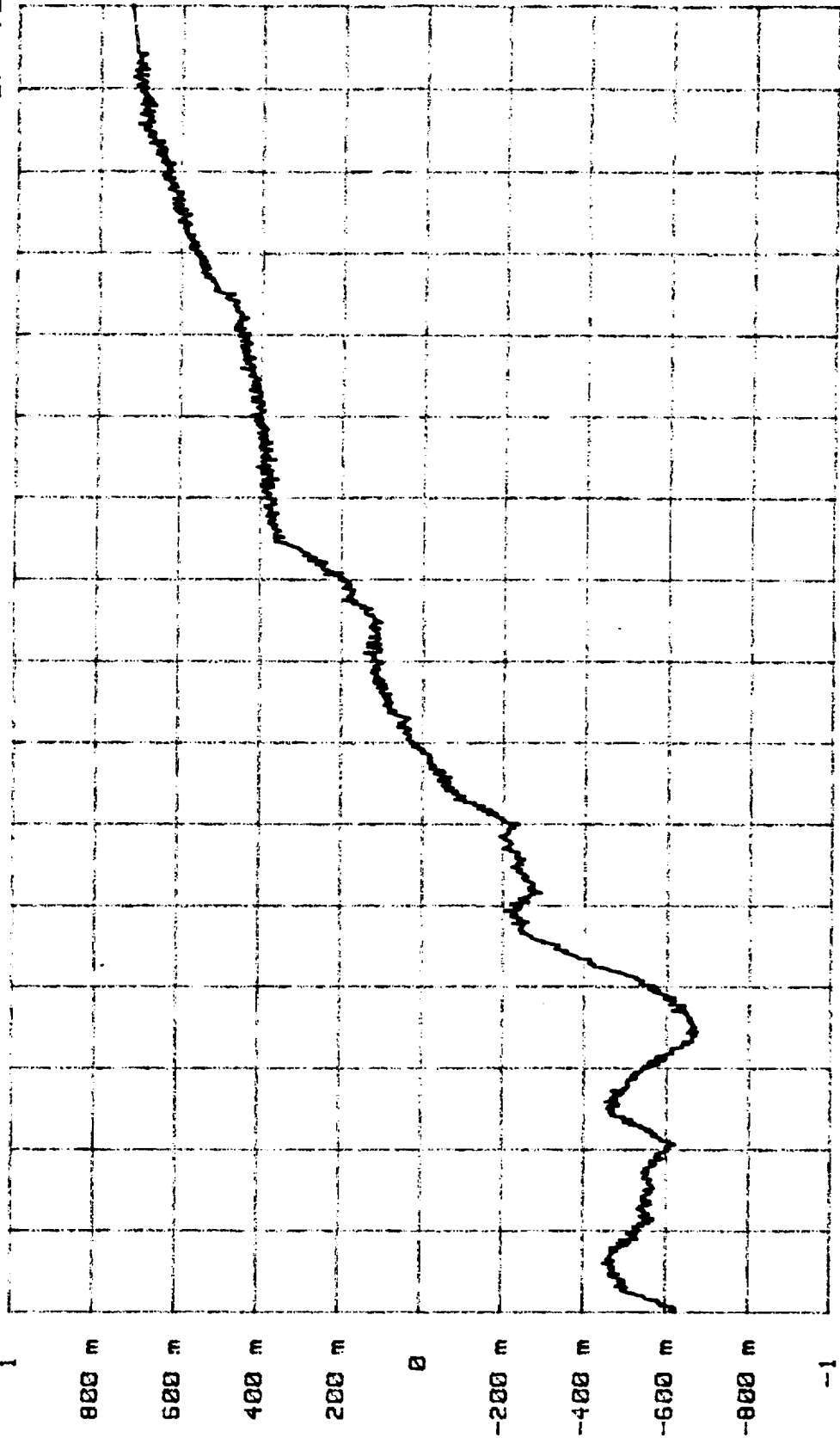


FIG. B5

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

CELL #1, SECOND ZERO DEG C TEST.

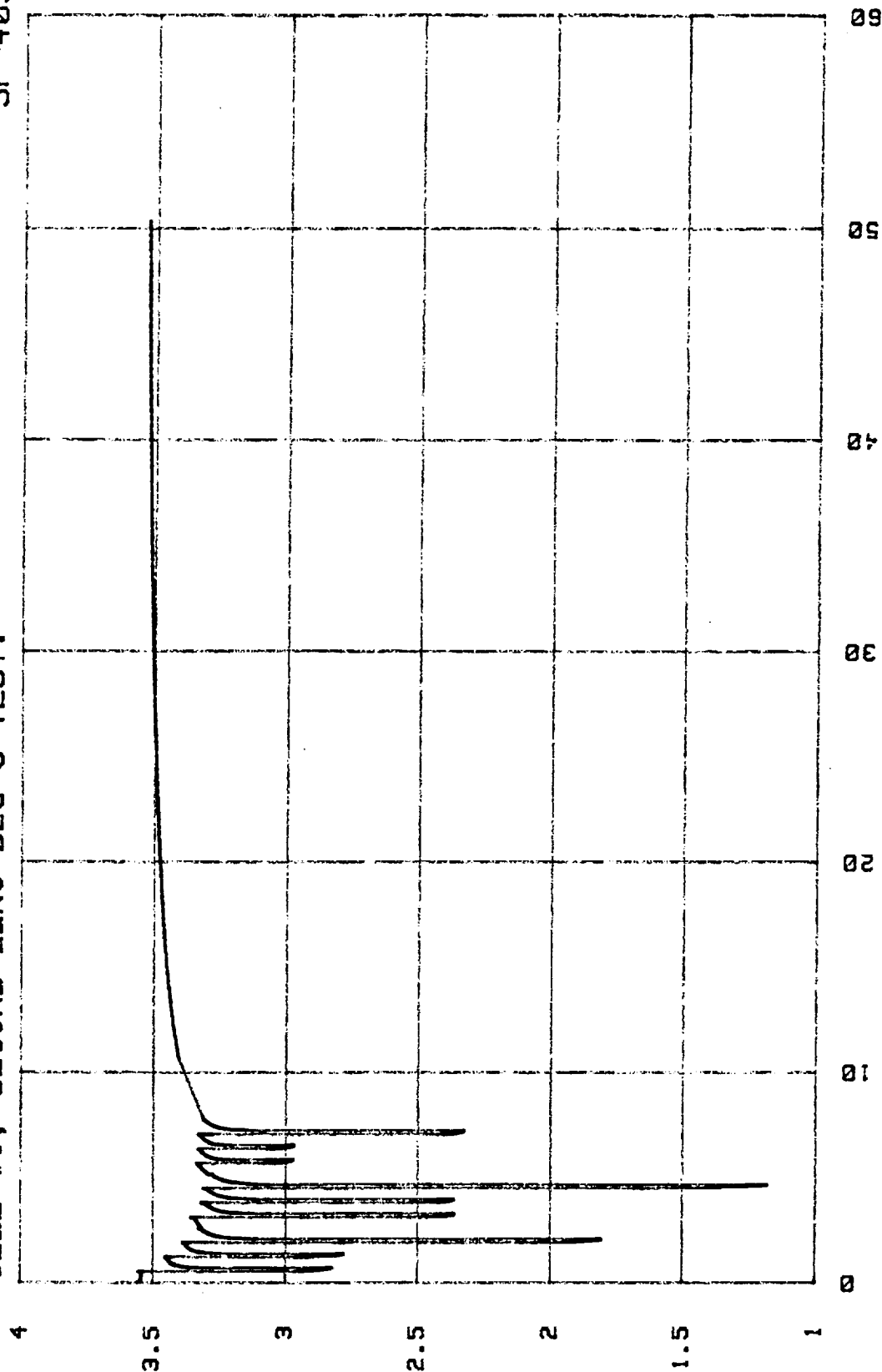


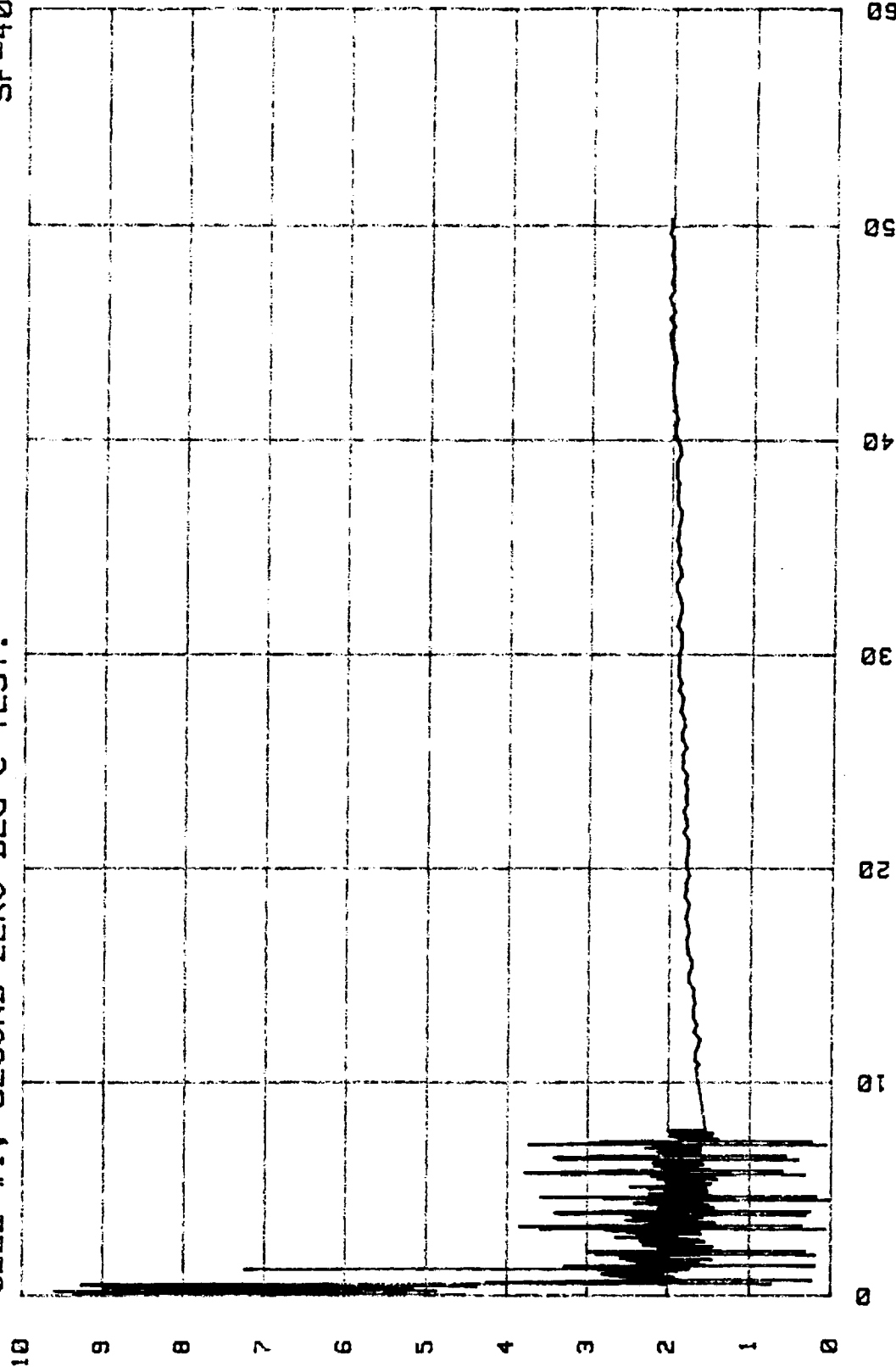
FIG. B6

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

CELL #1, SECOND ZERO DEG C TEST.



TIME (MINUTES)

CELL1_DCH B: Channel 3

FIG. B7

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

1 Dec 1995
SF-409

CELL #1, SECOND ZERO DEG C TEST.

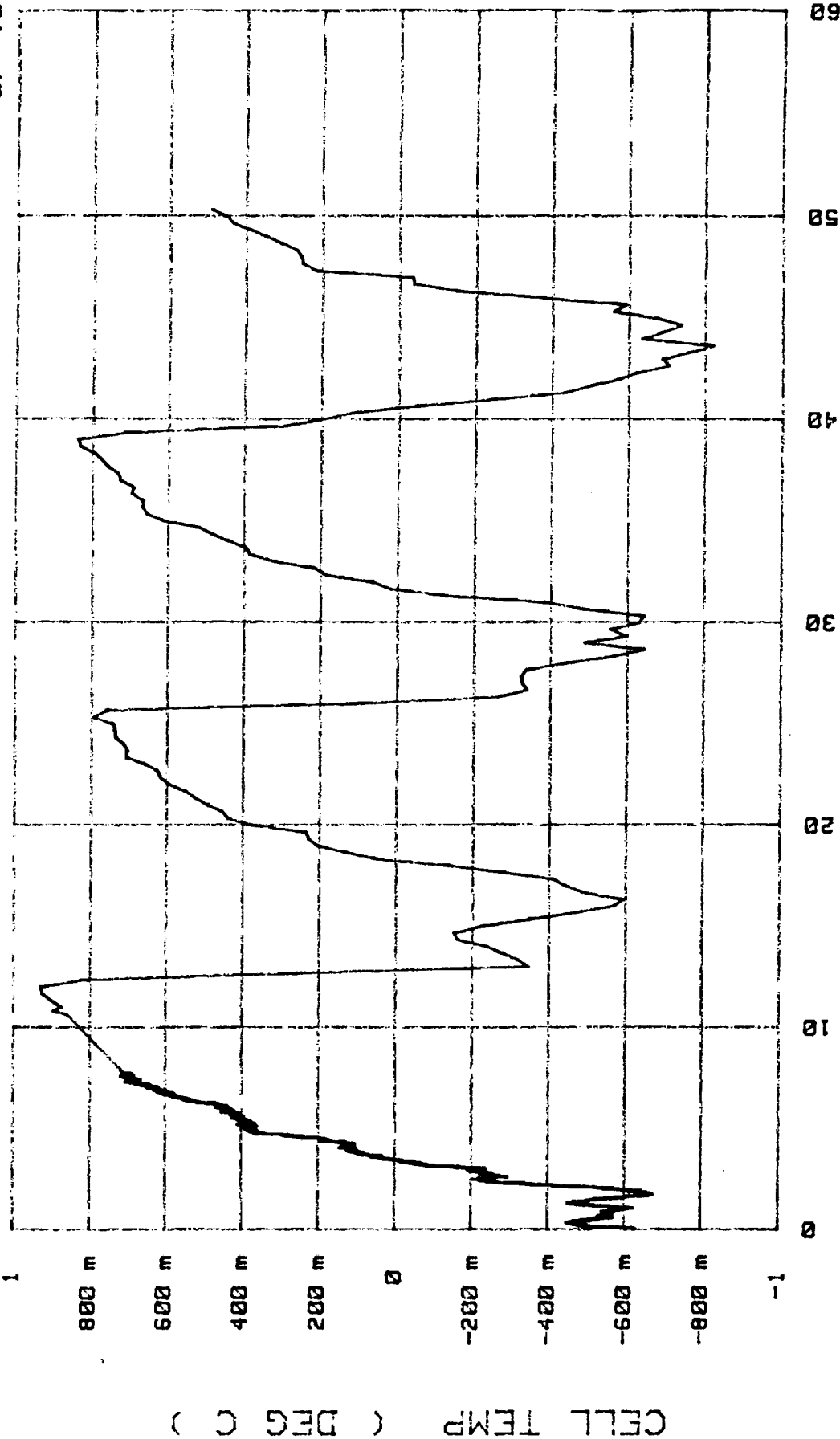


FIG. C1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

4 Dec 1995
SF-409

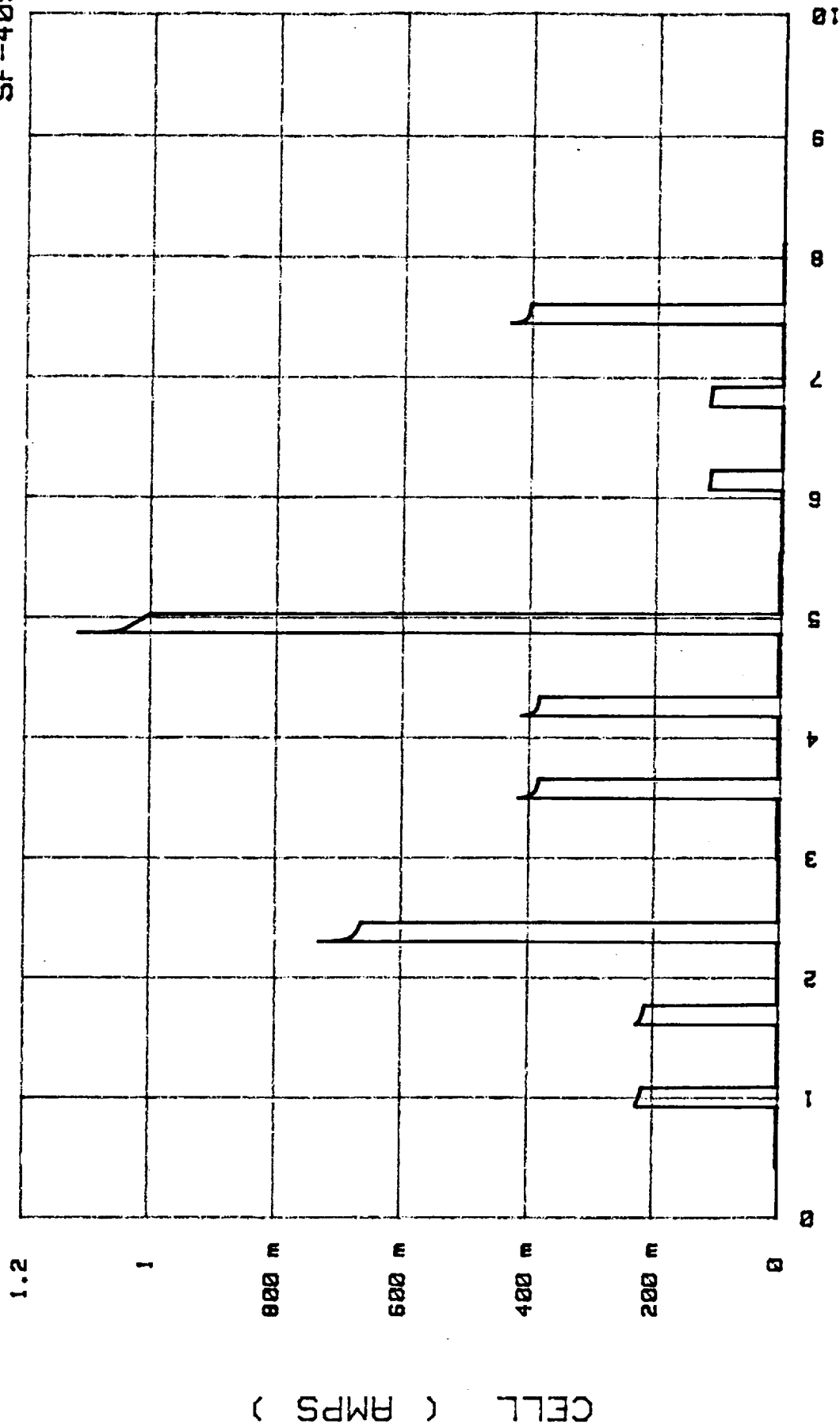


FIG. C2

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

4 Dec 1995
SF-409

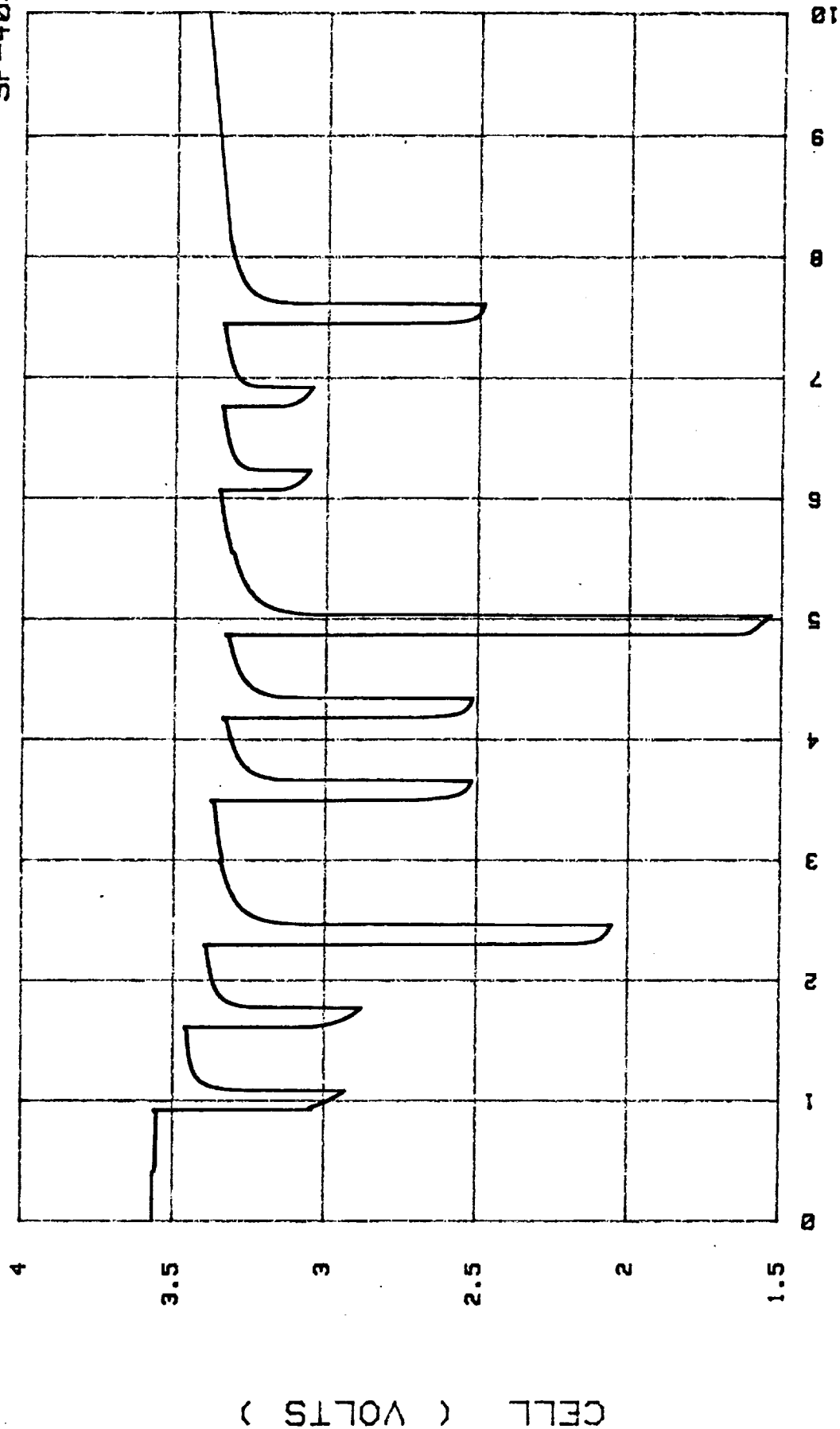


FIG. C3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

4 Dec 1995
SF-409

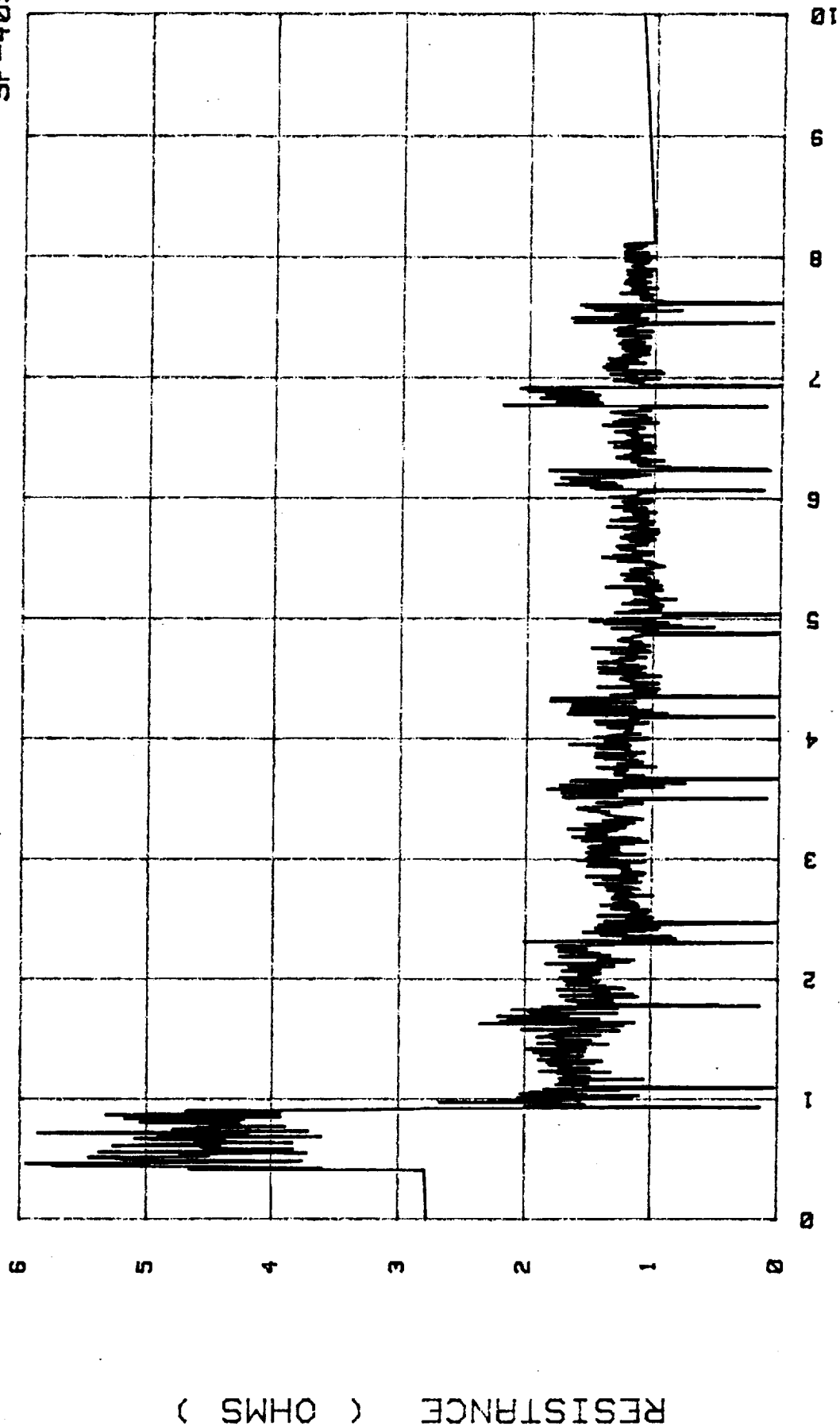


FIG. C4

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

4 Dec 1995
SF-409

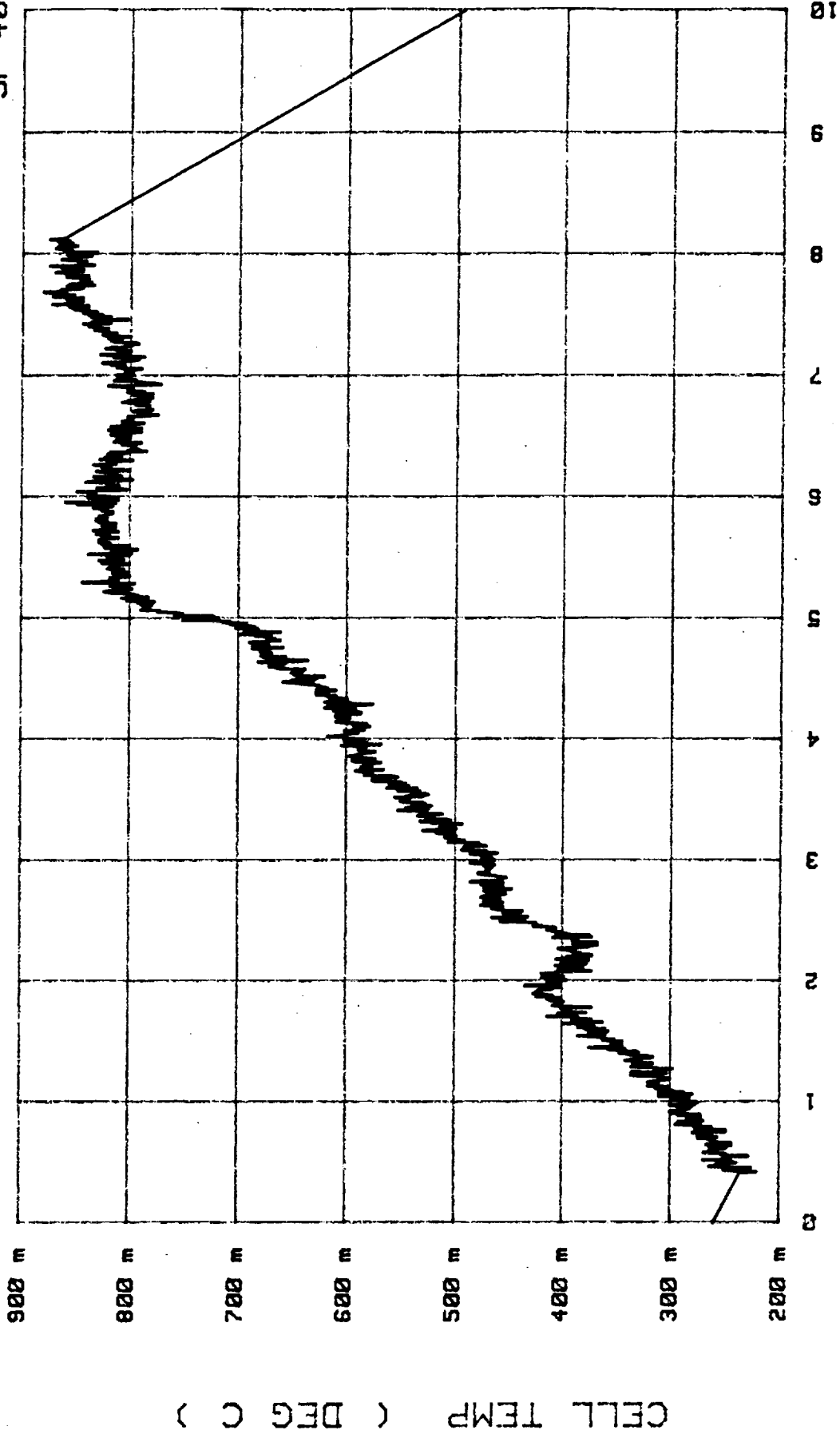
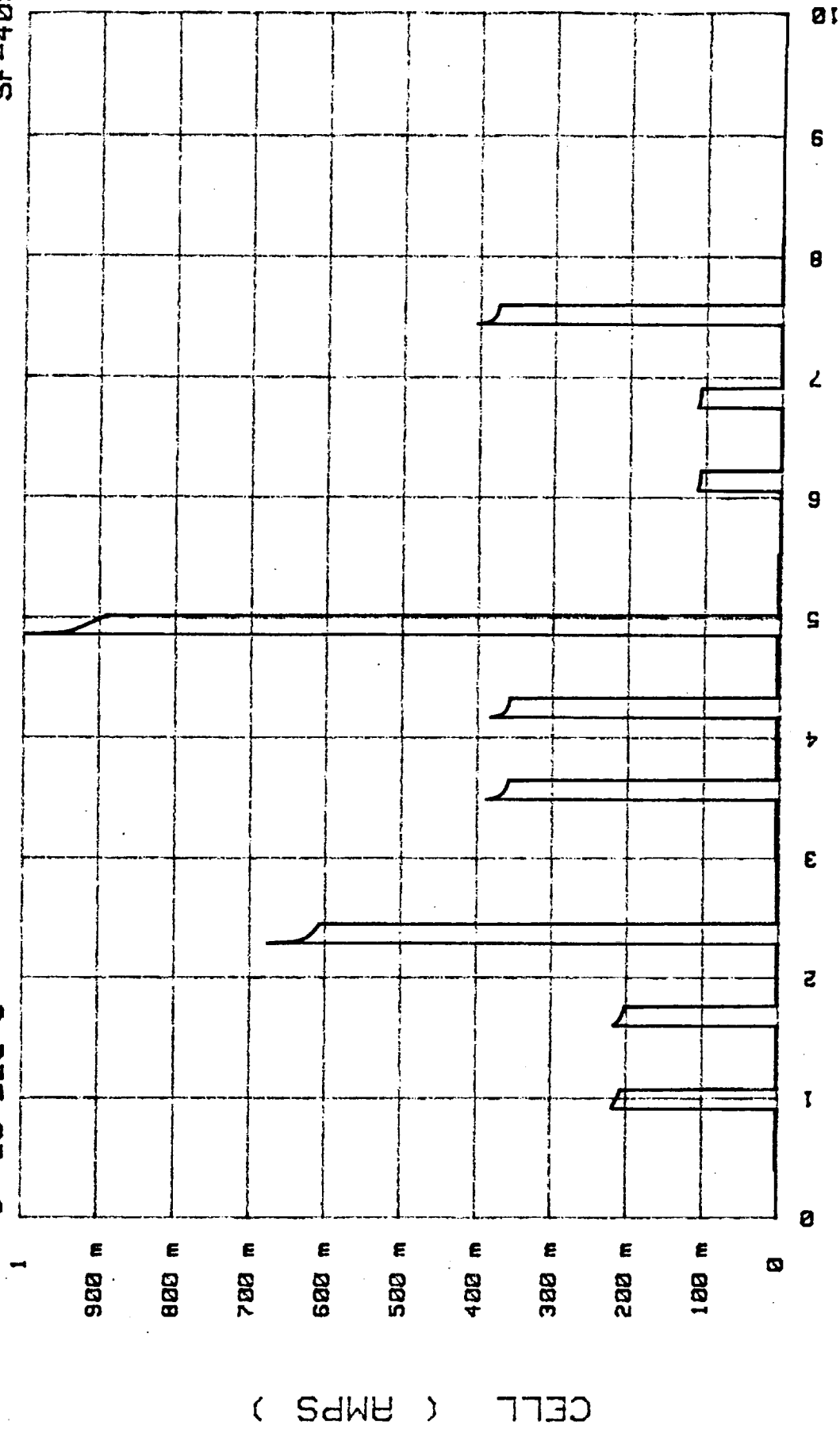


FIG. D1

Li/SOC12 CELL PERFORMANCE TEST

● -20 DEG C
CELL #1
4 Dec 1995
SF-409



TIME (MINUTES)

CELL1_DCH_D: Channel 1

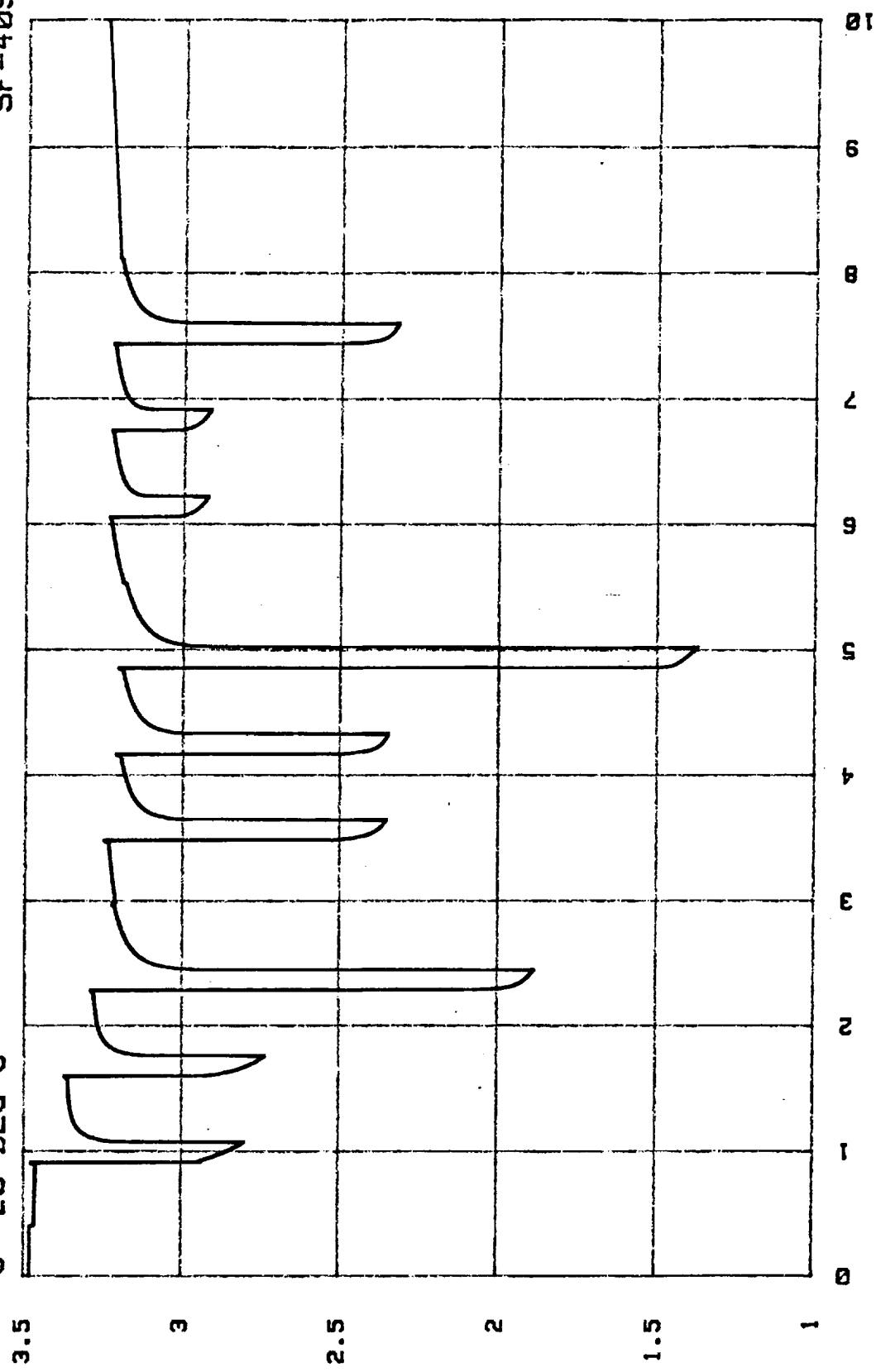
FIG. D2

Li/SOC12 CELL PERFORMANCE TEST

4 Dec 1995
SF-409

CELL #1

-20 DEG C



TIME (MINUTES)

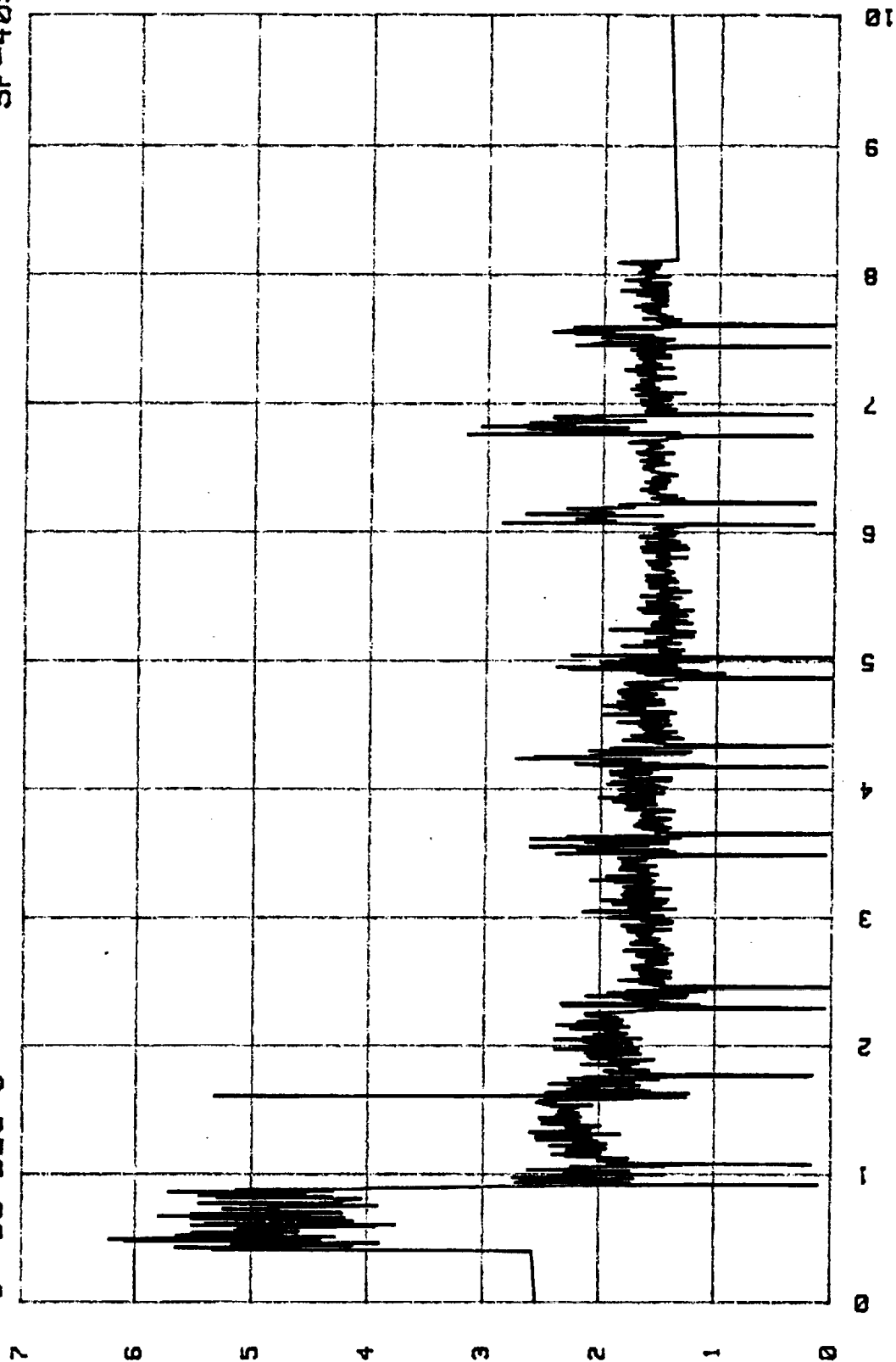
Fig. D3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

4 Dec 1995
SF-409

● -20 DEG C



TIME (MINUTES)

CELL1_DCH_D: Channel 3

FIG. D4

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

4 Dec 1995
SF-409

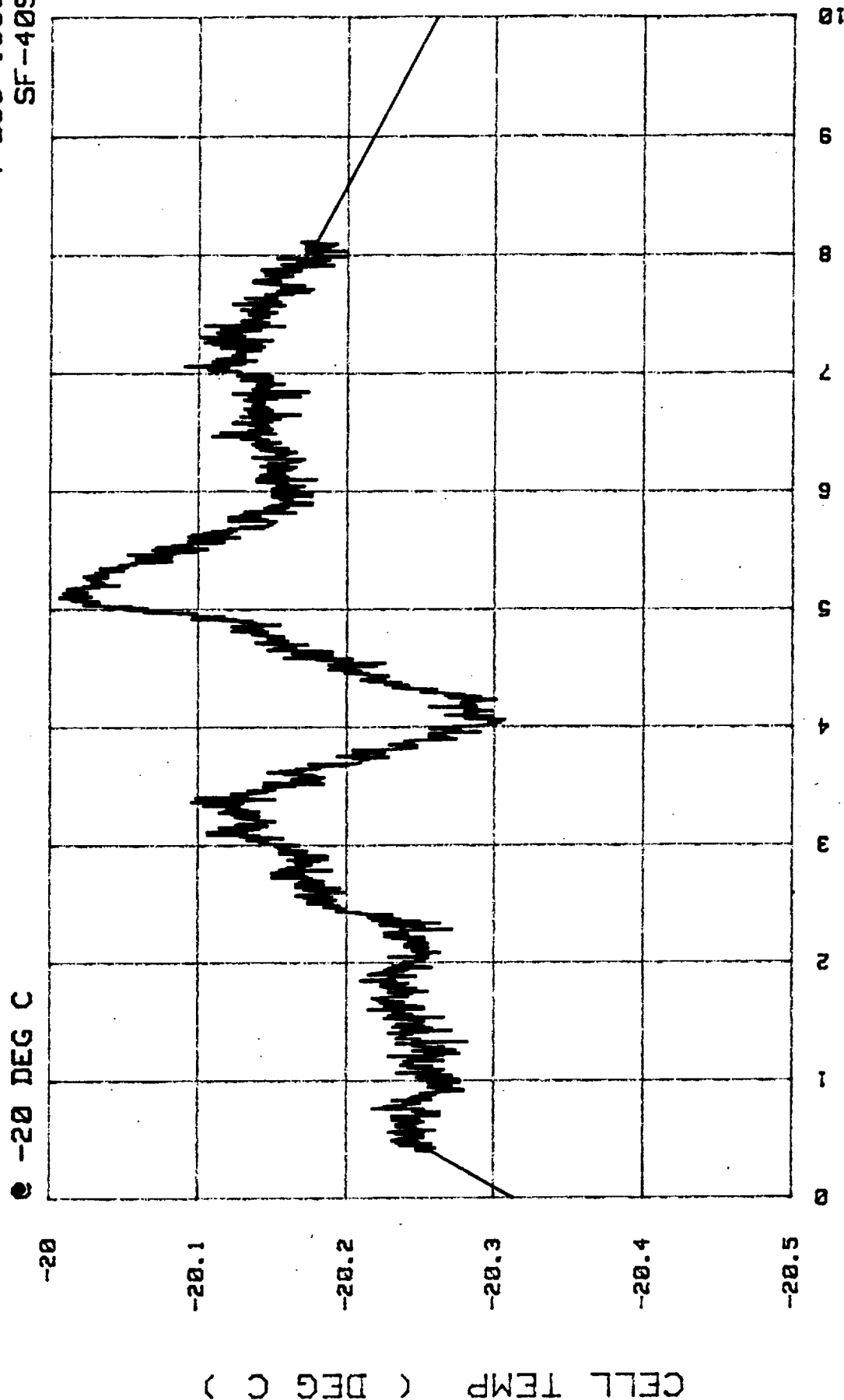


FIG. E1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

• -30 DEG C

1

900 m

800 m

700 m

600 m

500 m

400 m

300 m

200 m

100 m

0

CELL (RMPs)

0

2

3

4

5

6

7

8

9

10

TIME (MINUTES)

CELL1_DCH E: Channel 1

FIG. E2

Li/SOCI2 CELL PERFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

-30 DEG C

3.5

3

2.5

2

1.5

1

CELL (VOLTS)

0

2

3

4

5

6

7

8

9

10

TIME (MINUTES)

CELL1_DCH_E: Channel 2

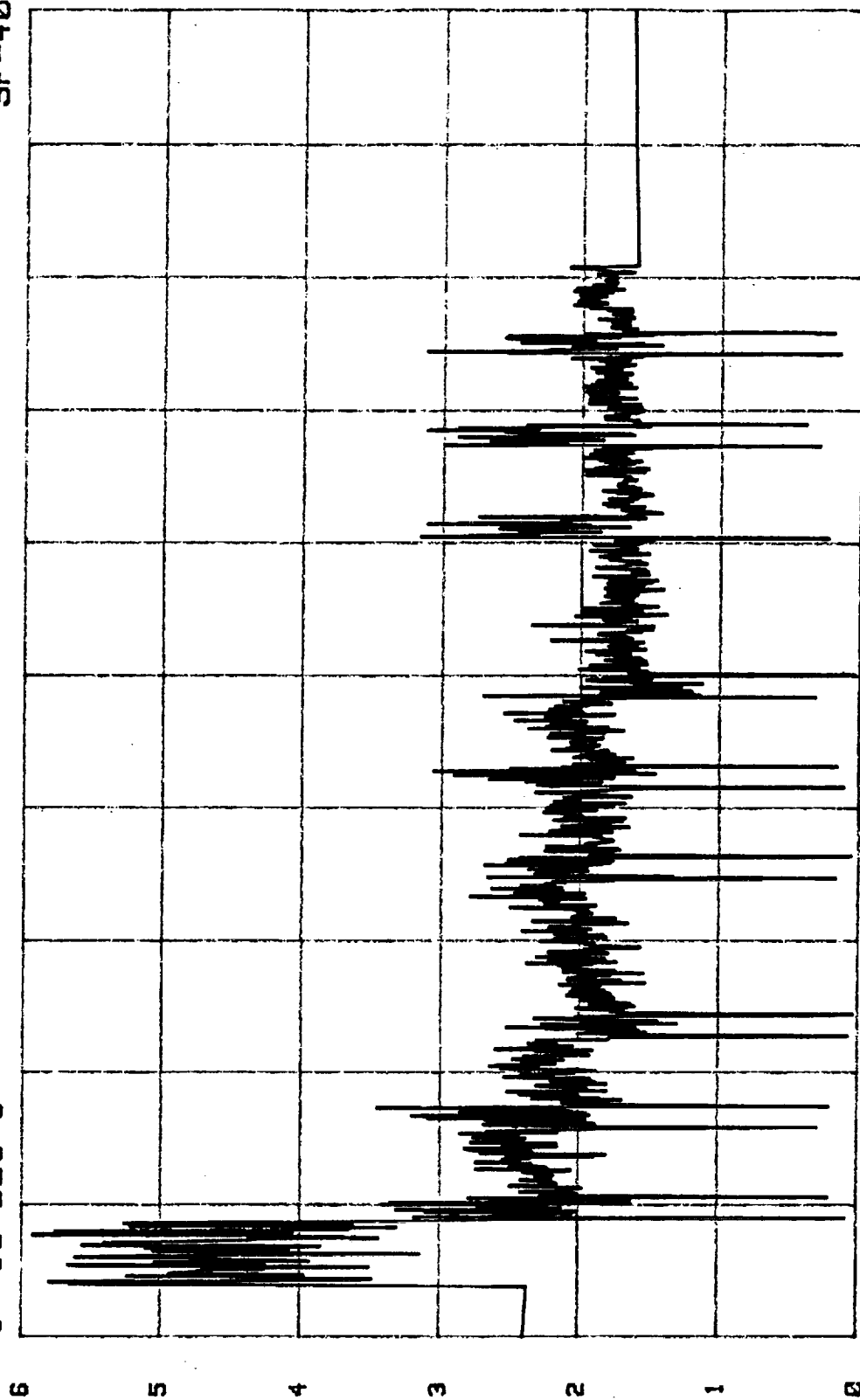
FIG. E 3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

● -30 DEG C



TIME (MINUTES)

FIG. E4

Li/SOC12 CELL PREFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

● -30 DEG C

CELL TEMP (DEG C)

Time (min)	Cell Temp (°C)
0	-30.65
1	-30.35
2	-30.40
3	-30.45
4	-30.40
5	-30.35
6	-30.30
7	-30.30
8	-30.30
9	-30.30
10	-30.30

10

6

8

2

9

5

4

3

2

1

0

TIME (MINUTES)

FIG. F1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

@ -40 DEG C

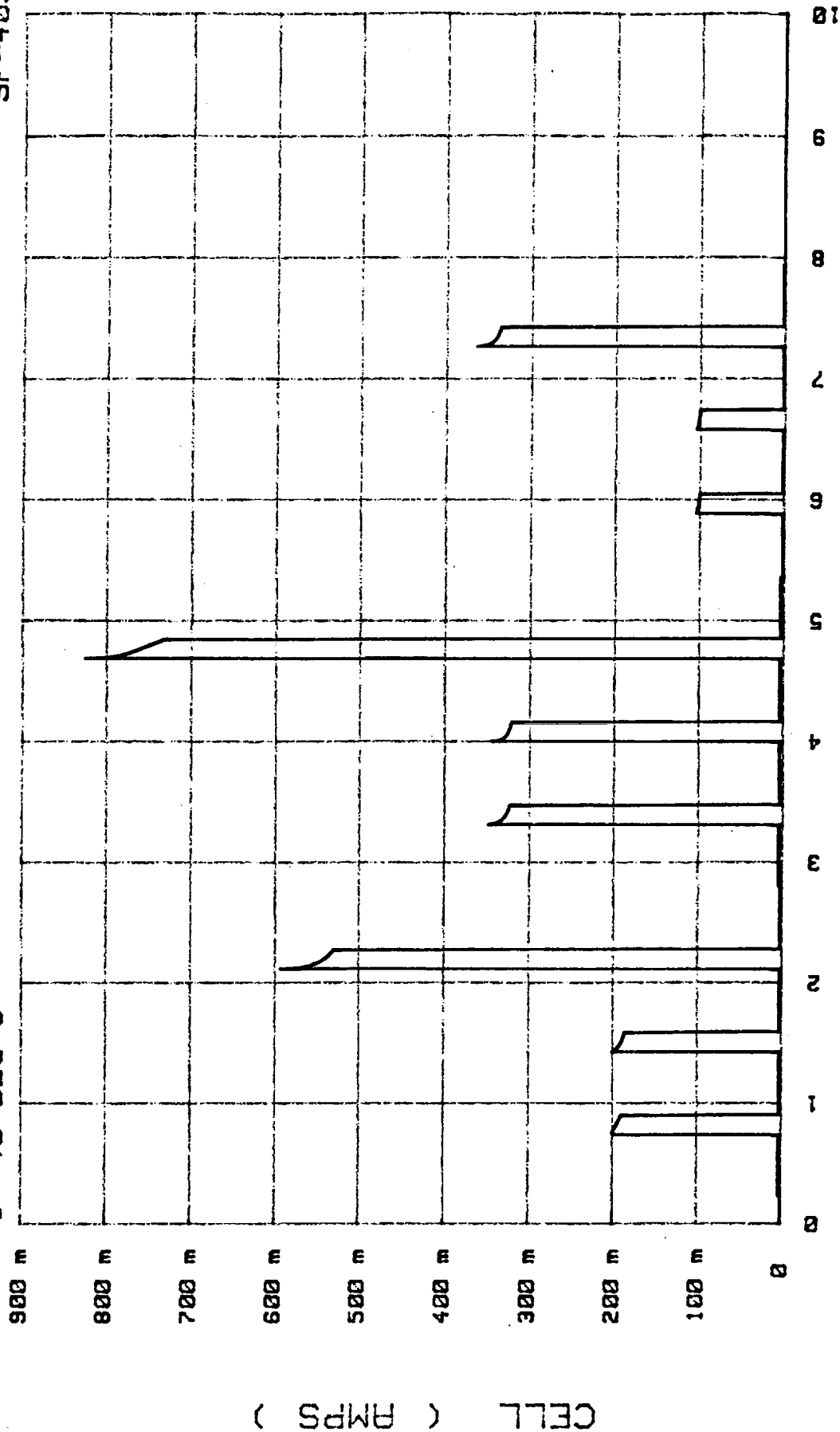


FIG. F2

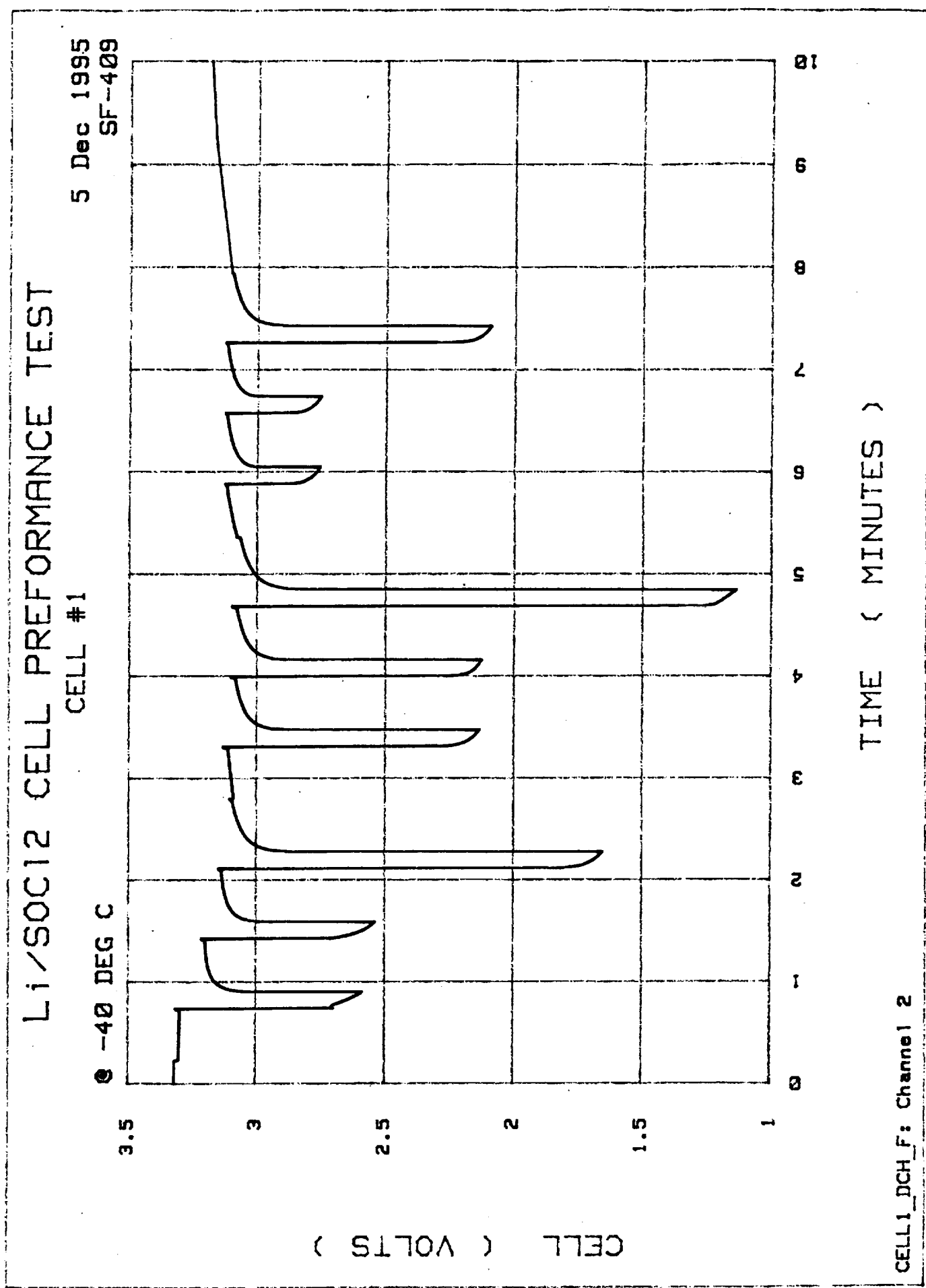


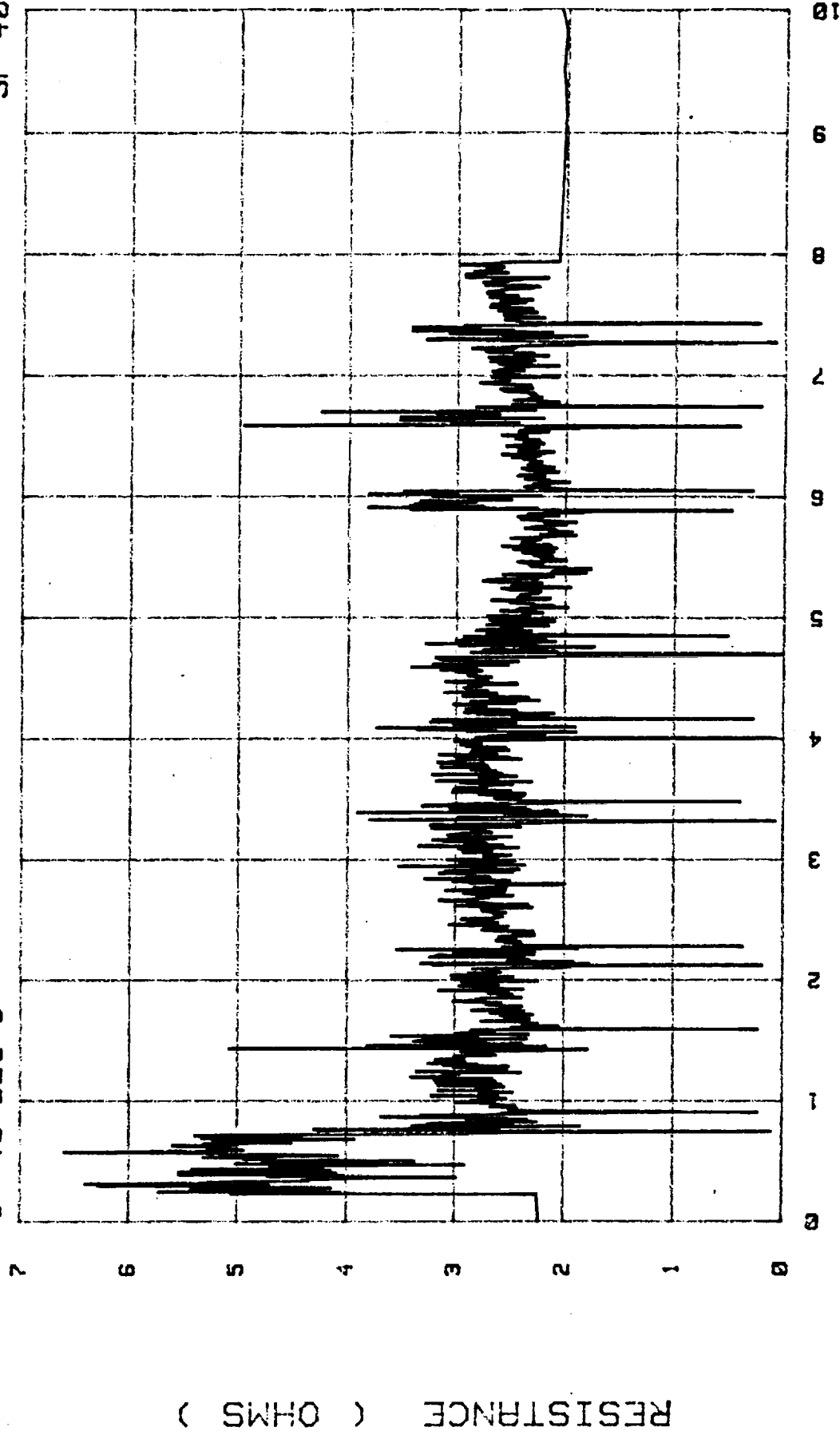
FIG. F3

Li/SOC12 CELL PREFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

@ -40 DEG C



TIME (MINUTES)

CELL1_DCH_F: Channel 3

FIG. F4

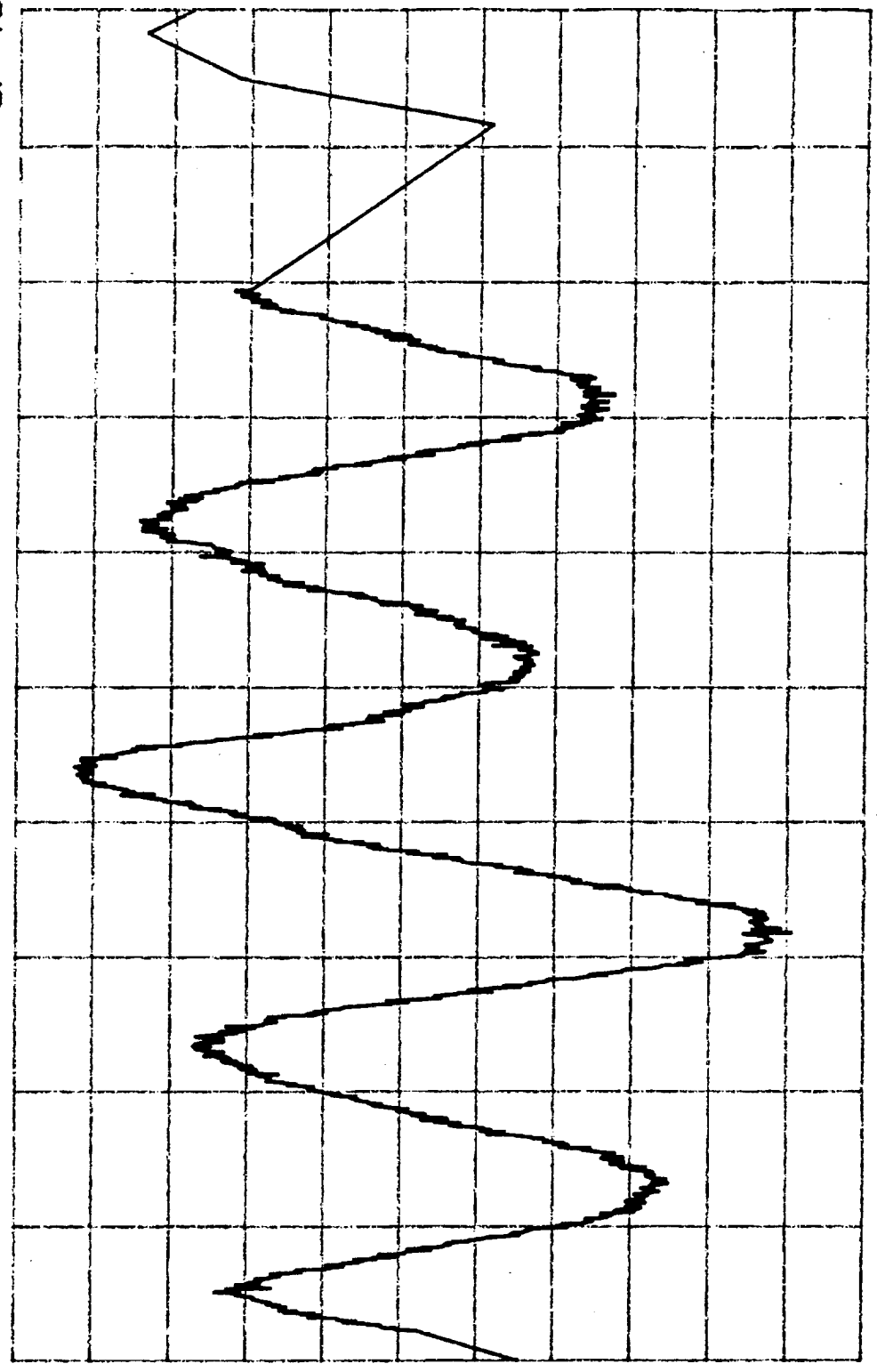
Li/SOC12 CELL PREFORMANCE TEST

5 Dec 1995
SF-409

CELL #1

0 -40 DEG C

CELL TEMP (DEG C)
-40.1
-40.2
-40.3
-40.4
-40.5
-40.6
-40.7
-40.8
-40.9
-41
-41.1
-41.2



TIME (MINUTES)
0
1
2
3
4
5
6
7
8
9
10

FIG. G1

Li/SOC12 CELL PERFORMANCE TEST

5 Dec 1995
SF-409

CELL #1

@ -50 DEG C

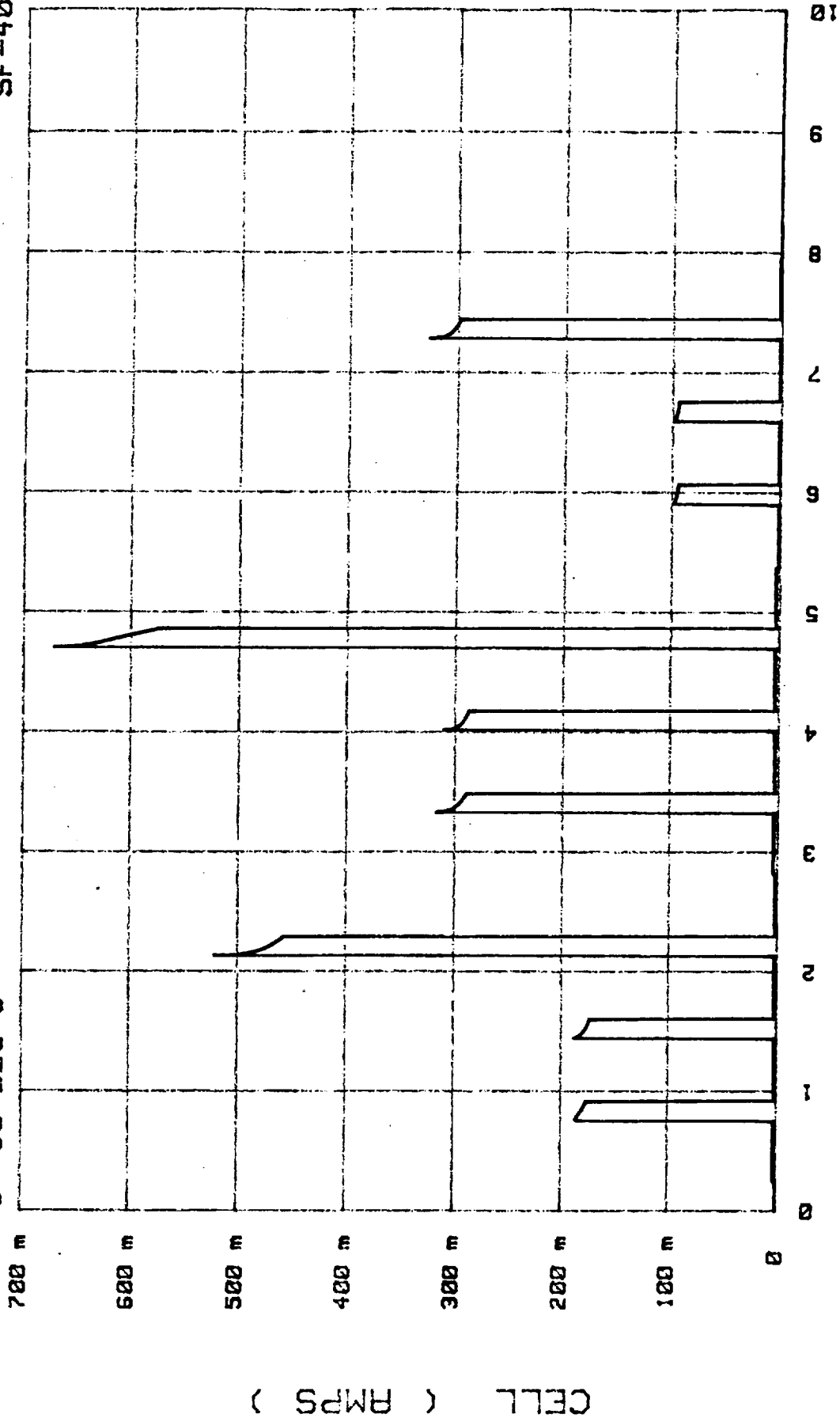


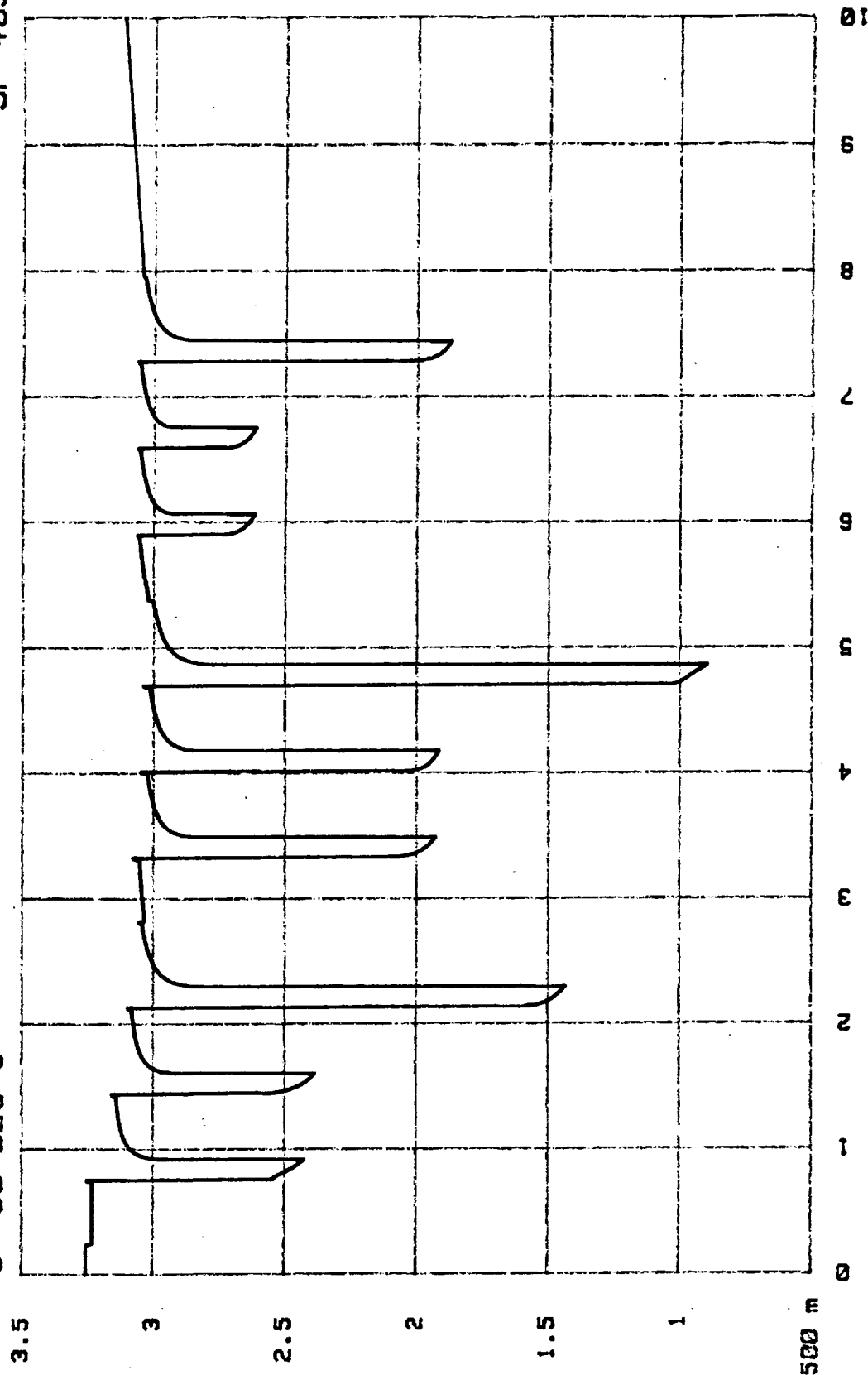
FIG. G2

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

② -50 DEG C



TIME (MINUTES)

CELL1_DCH_G: Channel 2

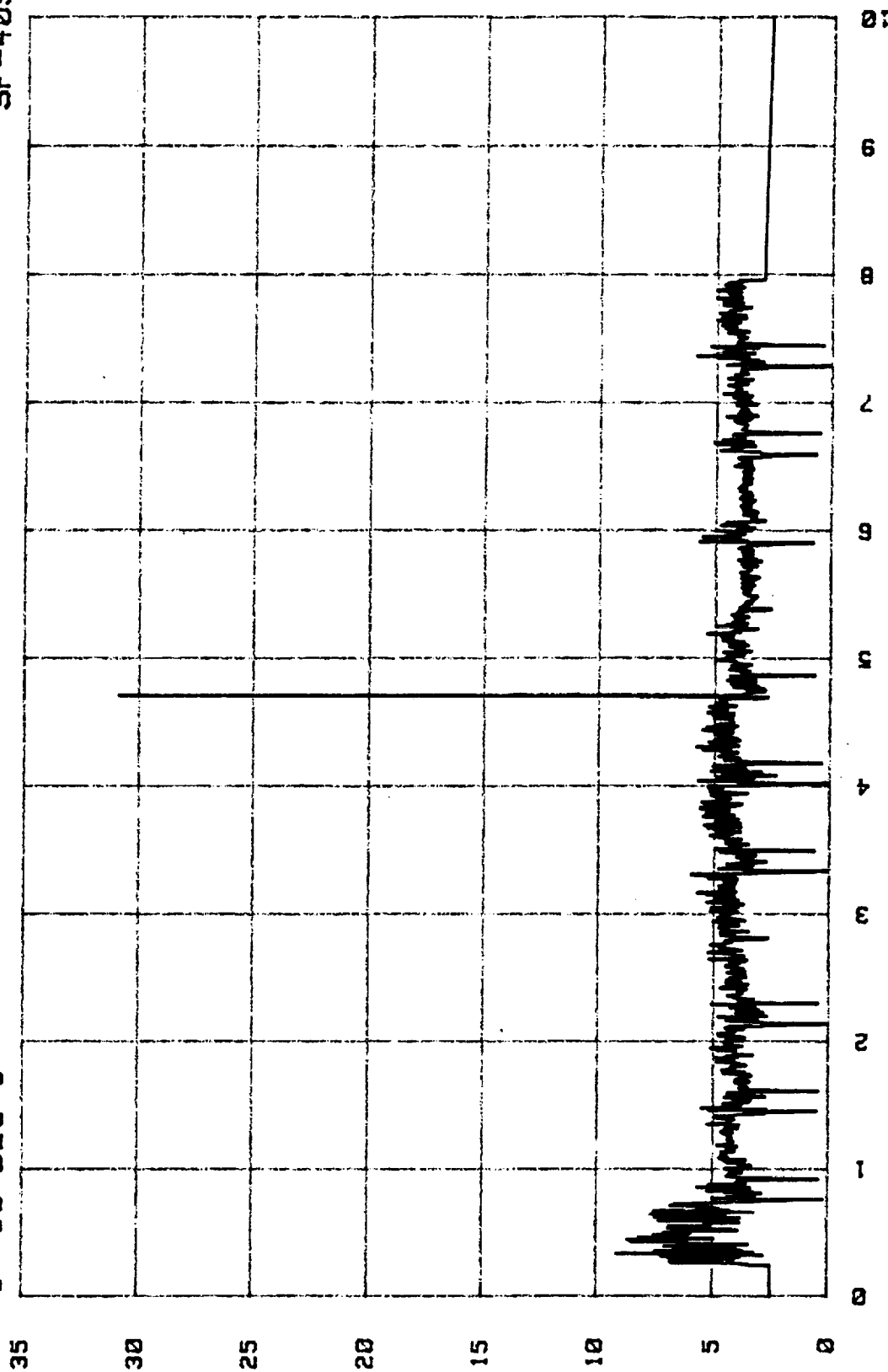
FIG. G3

Li/SOC12 CELL PREFORMANCE TEST

CELL #1

5 Dec 1995
SF-409

@ -50 DEG C



RESISTANCE (OHMS)

TIME (MINUTES)

FIG. G4

Li/SOC12 CELL PERFORMANCE TEST

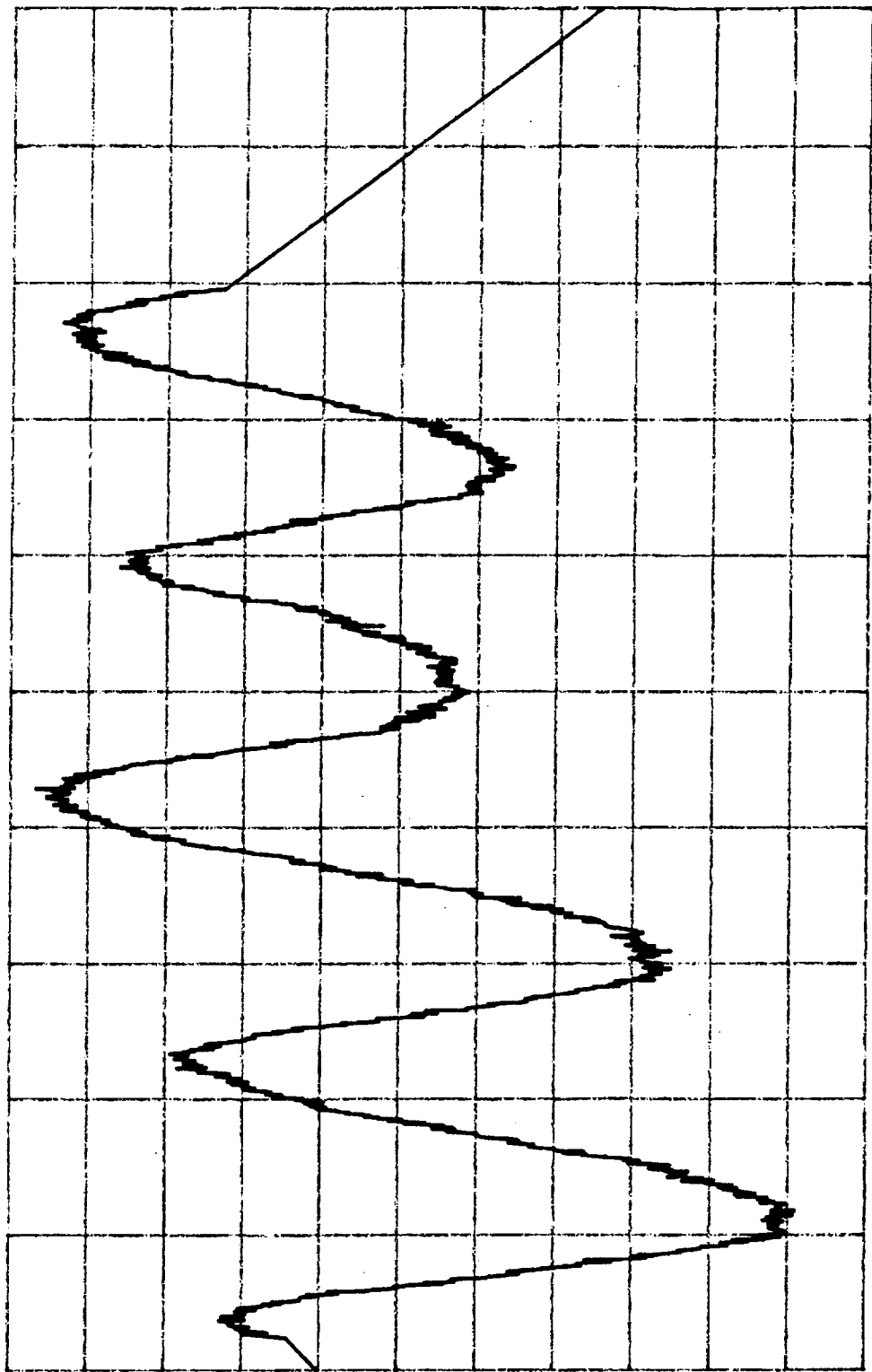
CELL #1

5 Dec 1995
SF-409

● -50 DEG C

CELL TEMP (DEG C)

-50.8
-50.9
-51
-51.1
-51.2
-51.3
-51.4
-51.5
-51.6
-51.7
-51.8
-51.9



01

6

8

2

9

5

4

3

2

1

0

TIME (MINUTES)

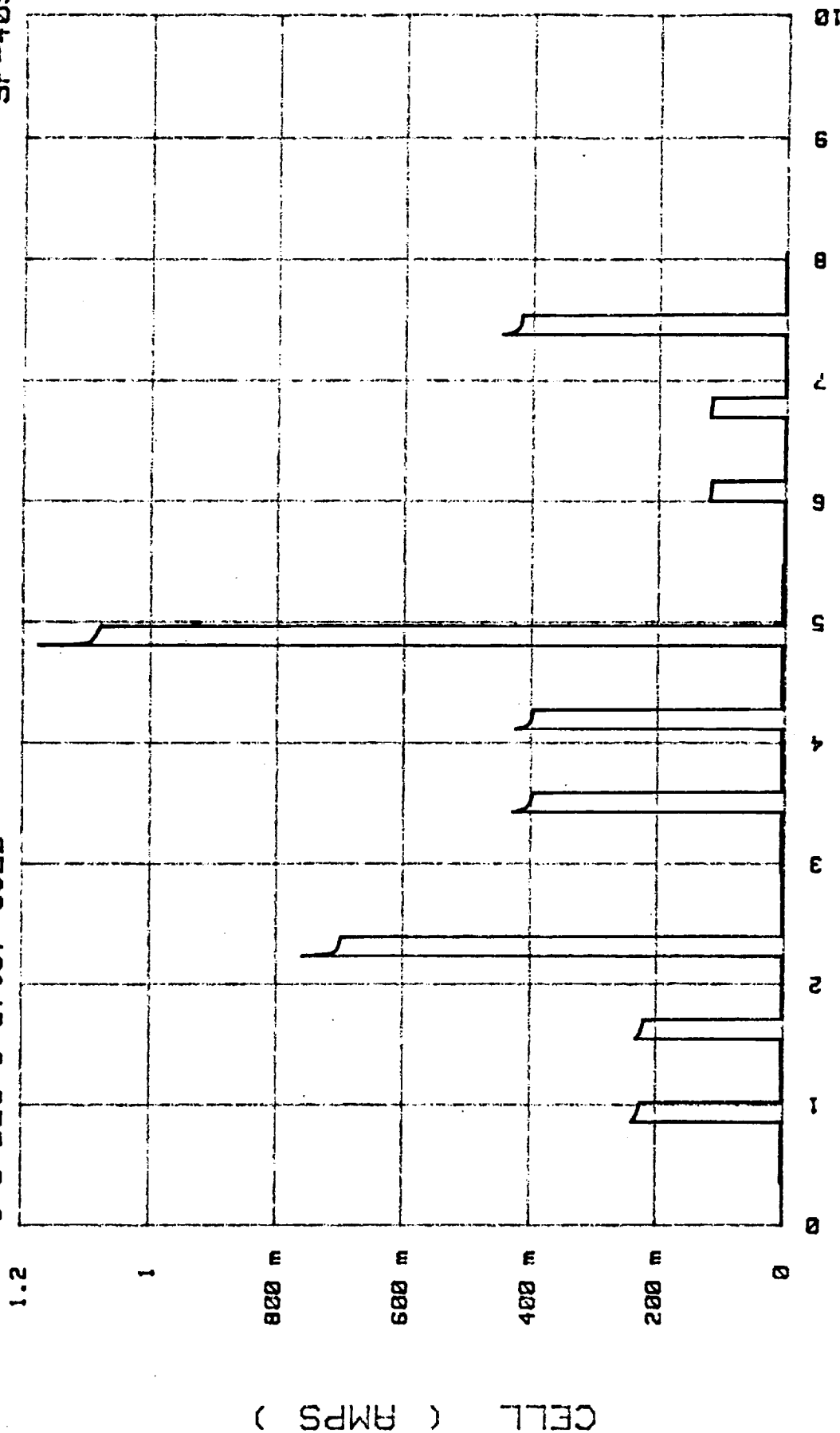
FIG. H1

Li/SOC12 CELL PREFORMANCE TEST

6 Dec 1995
SF-409

CELL #1

0 DEG C after COLD



TIME (MINUTES)

CELL1_DCH_H: Channel 1

FIG. H2

Li/SOCI2 CELL PERFORMANCE TEST

6 Dec 1995
SF-409

CELL #1

0 DEG C after COLD

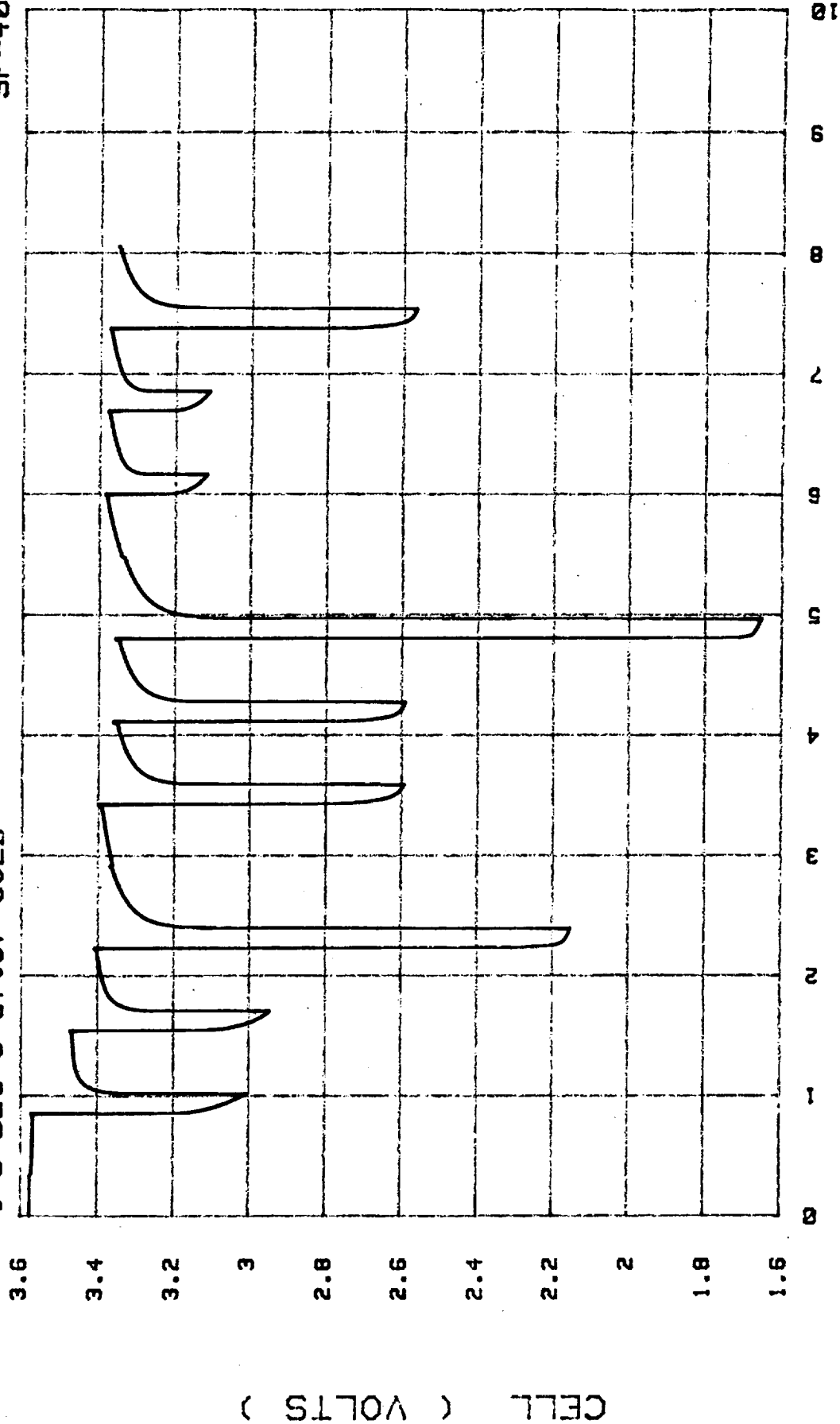


FIG. H3

Li/SOC12 CELL PREFORMANCE TEST

6 Dec 1995
SF-409

CELL #1

0 DEG C after COLD

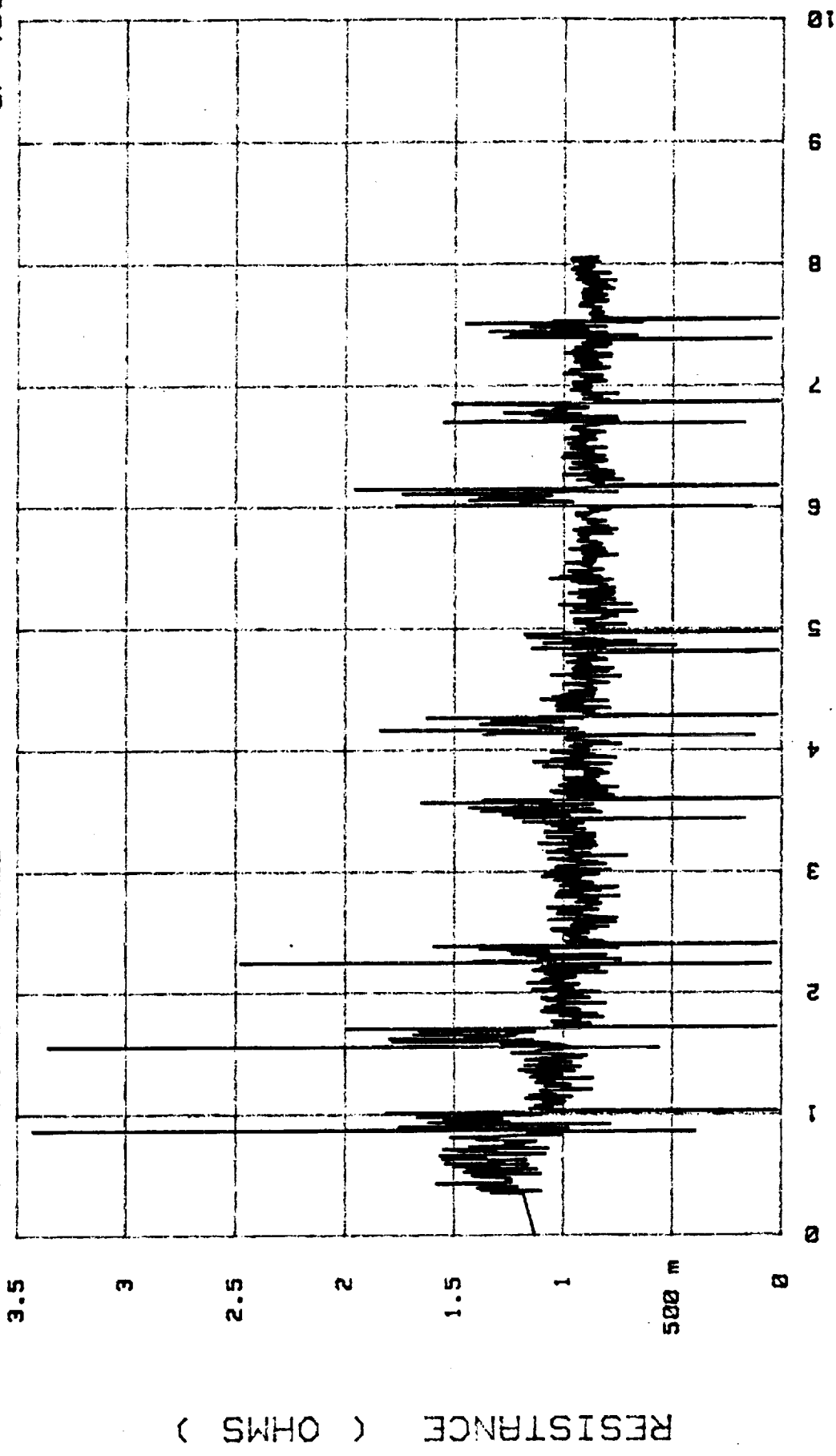


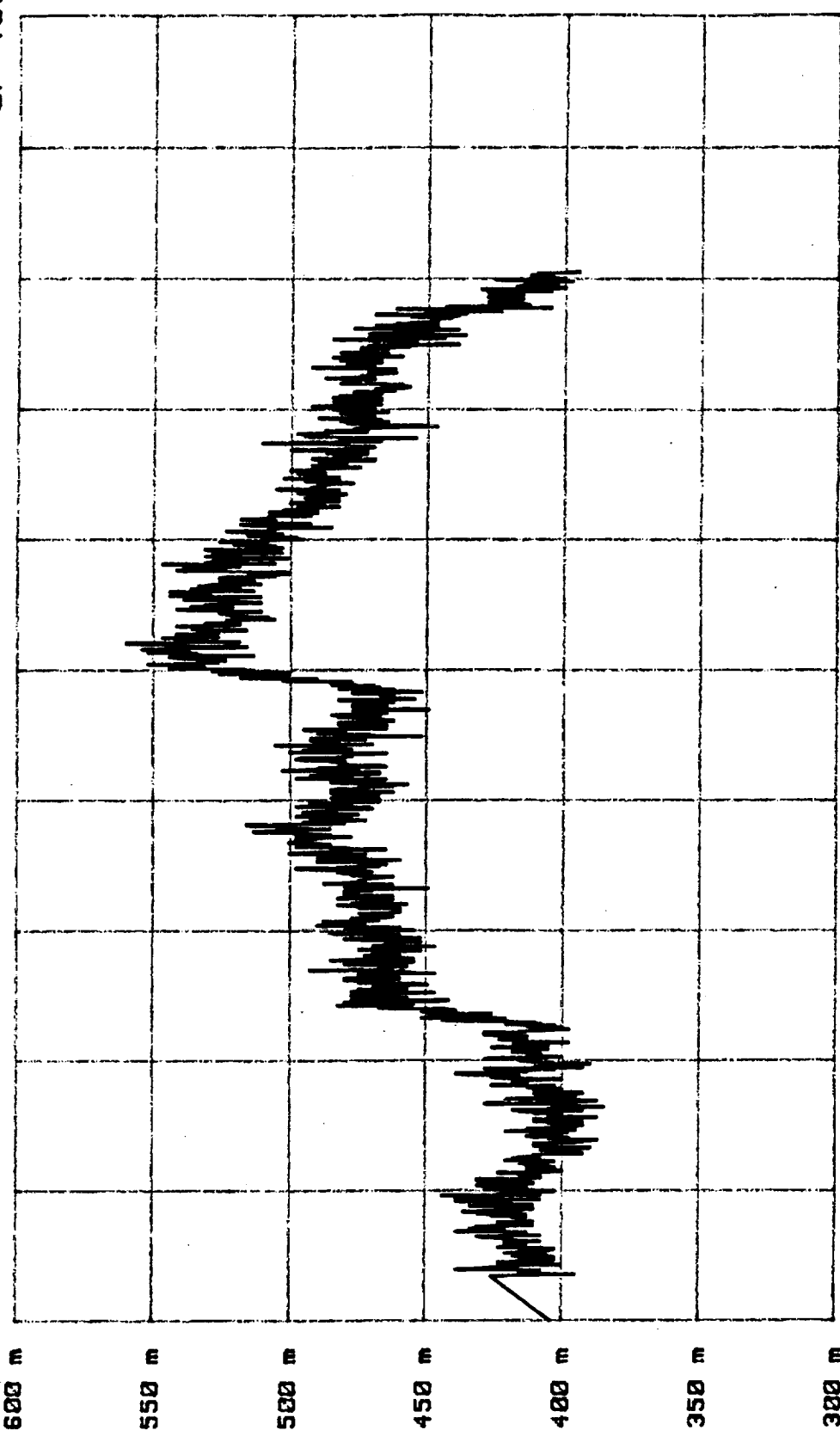
FIG. H4

Li/SOC12 CELL PERFORMANCE TEST

6 Dec 1995
SF-409

CELL #1

0 DEG C after COLD



TIME (MINUTES)

CELL1_DCH_H: Channel 4

FIG. I 1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

6 Dec 1995
SF-409

+ 20°C

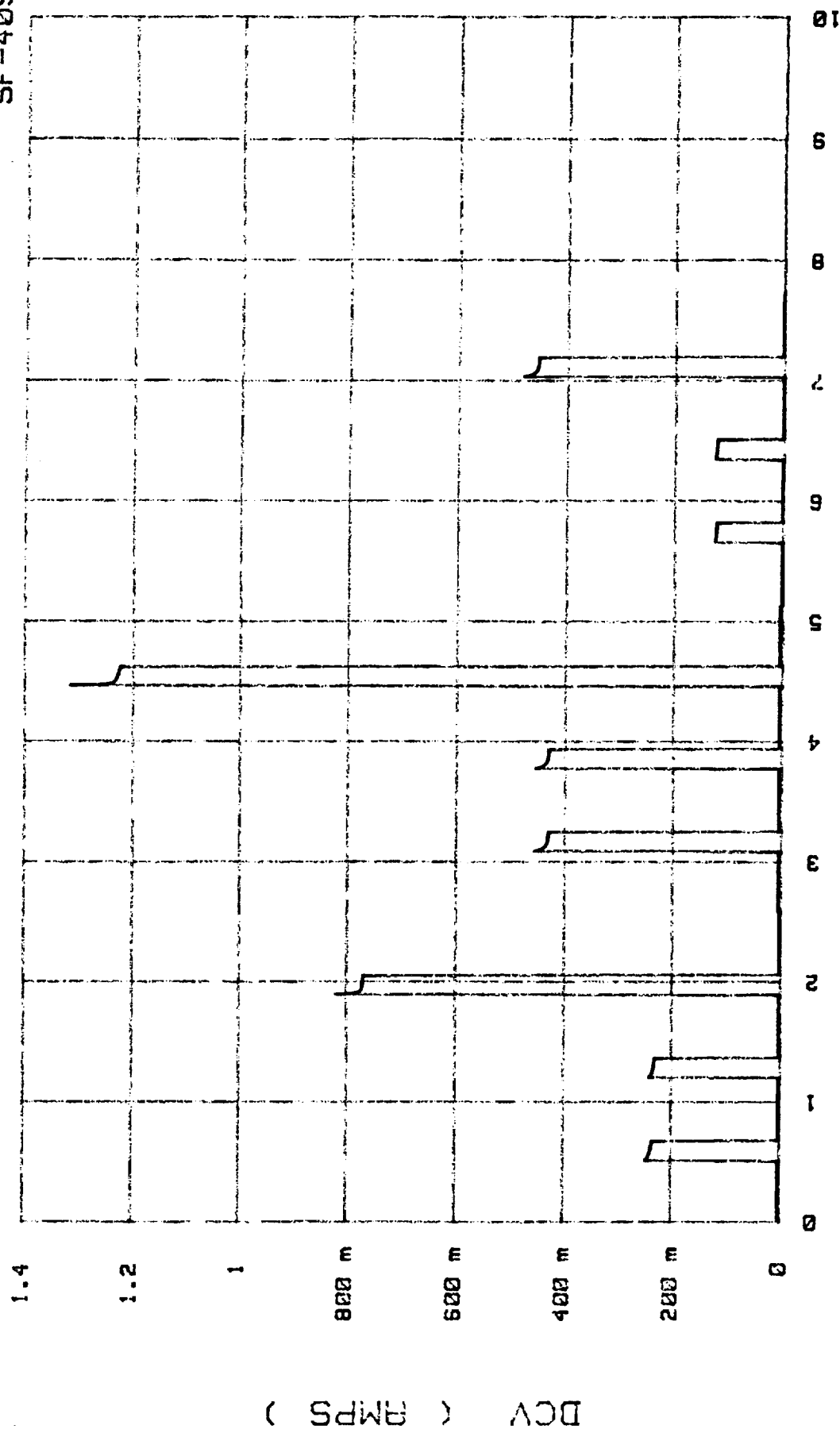


FIG. 12

Li/SOCI2 CELL PERFORMANCE TEST

CELL #1

6 Dec 1995
SF-409

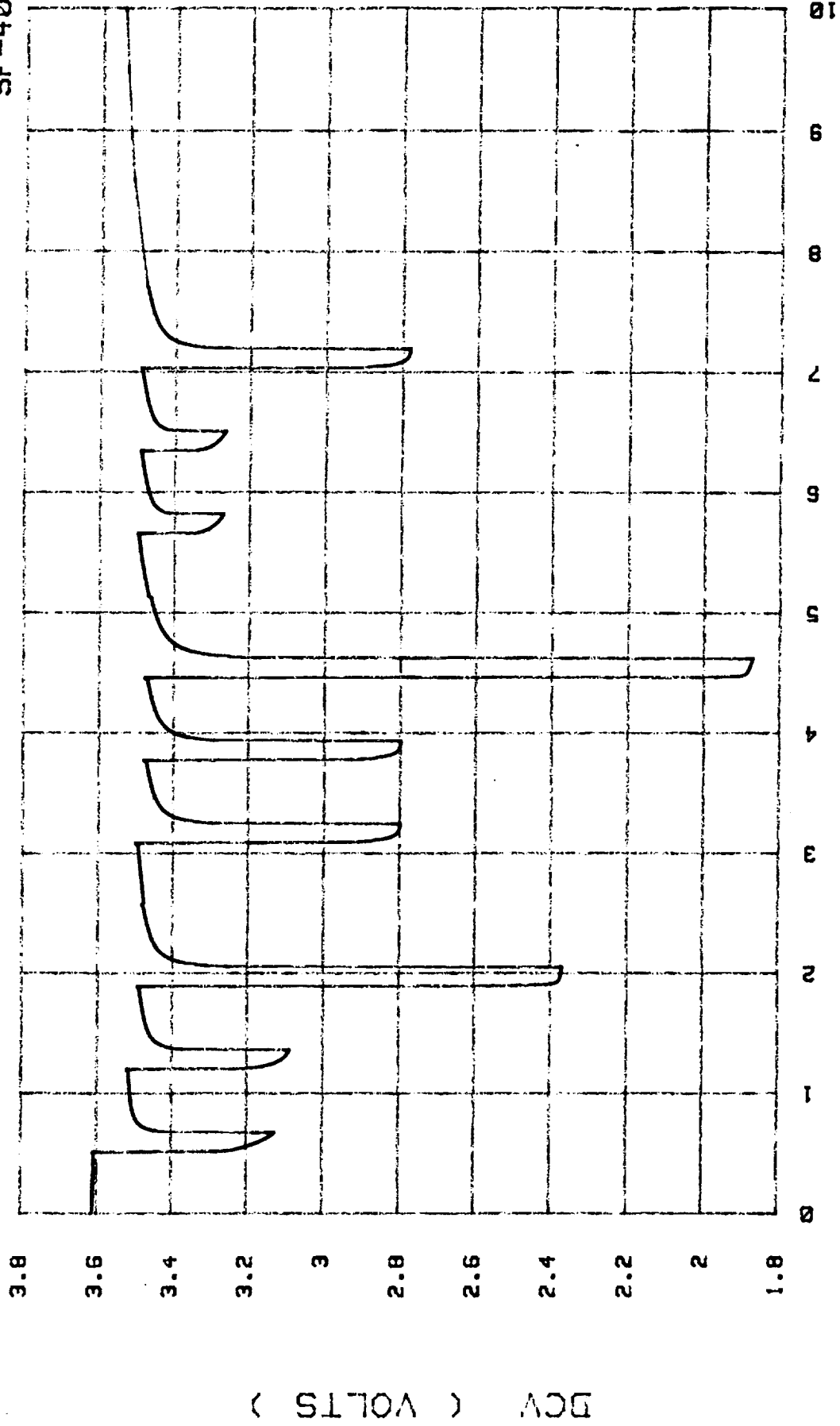


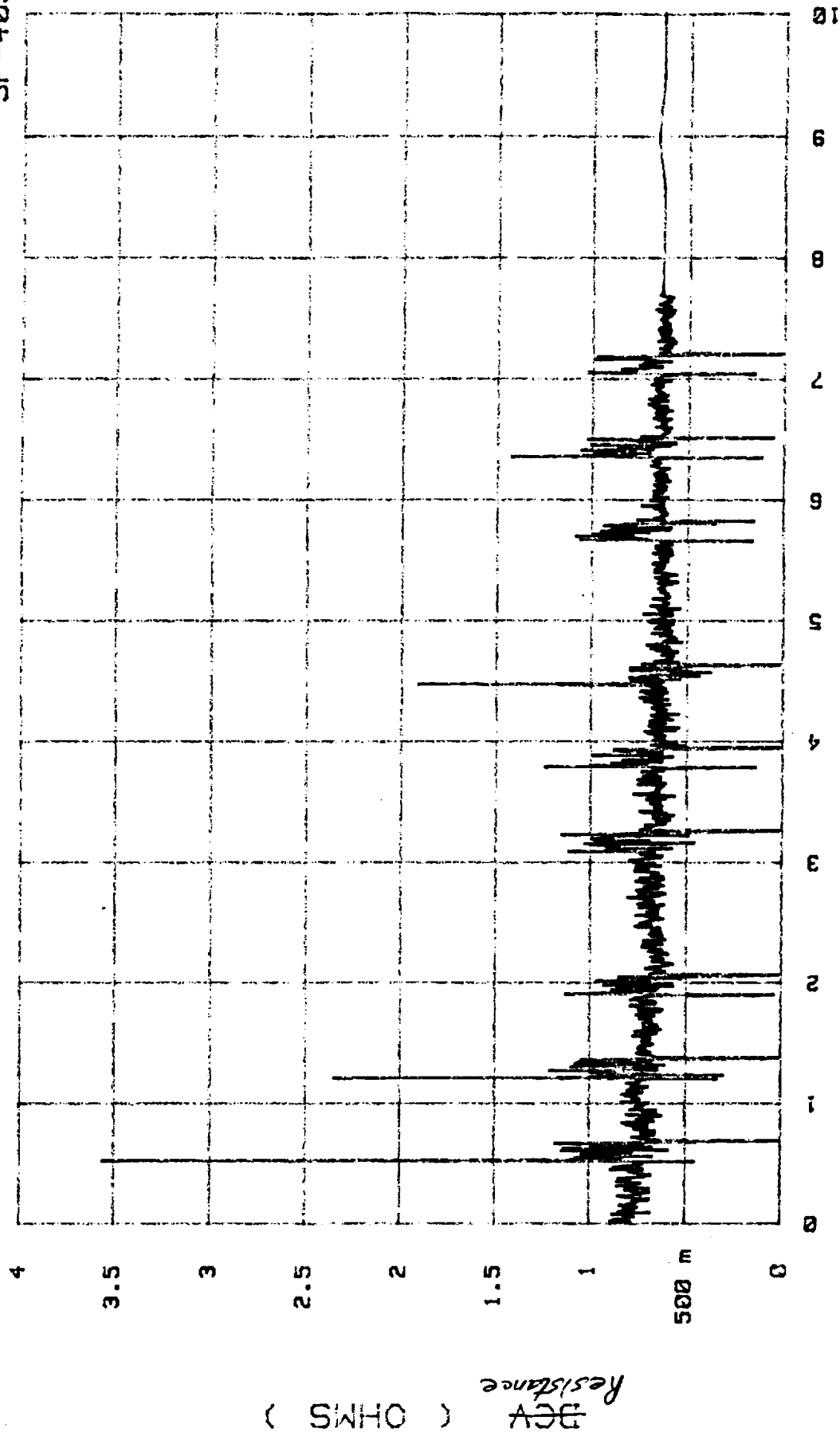
FIG. 13

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

6 Dec 1995

SF-409



TIME (MINUTES)

FIG. 14

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

6 Dec 1995
SF-409

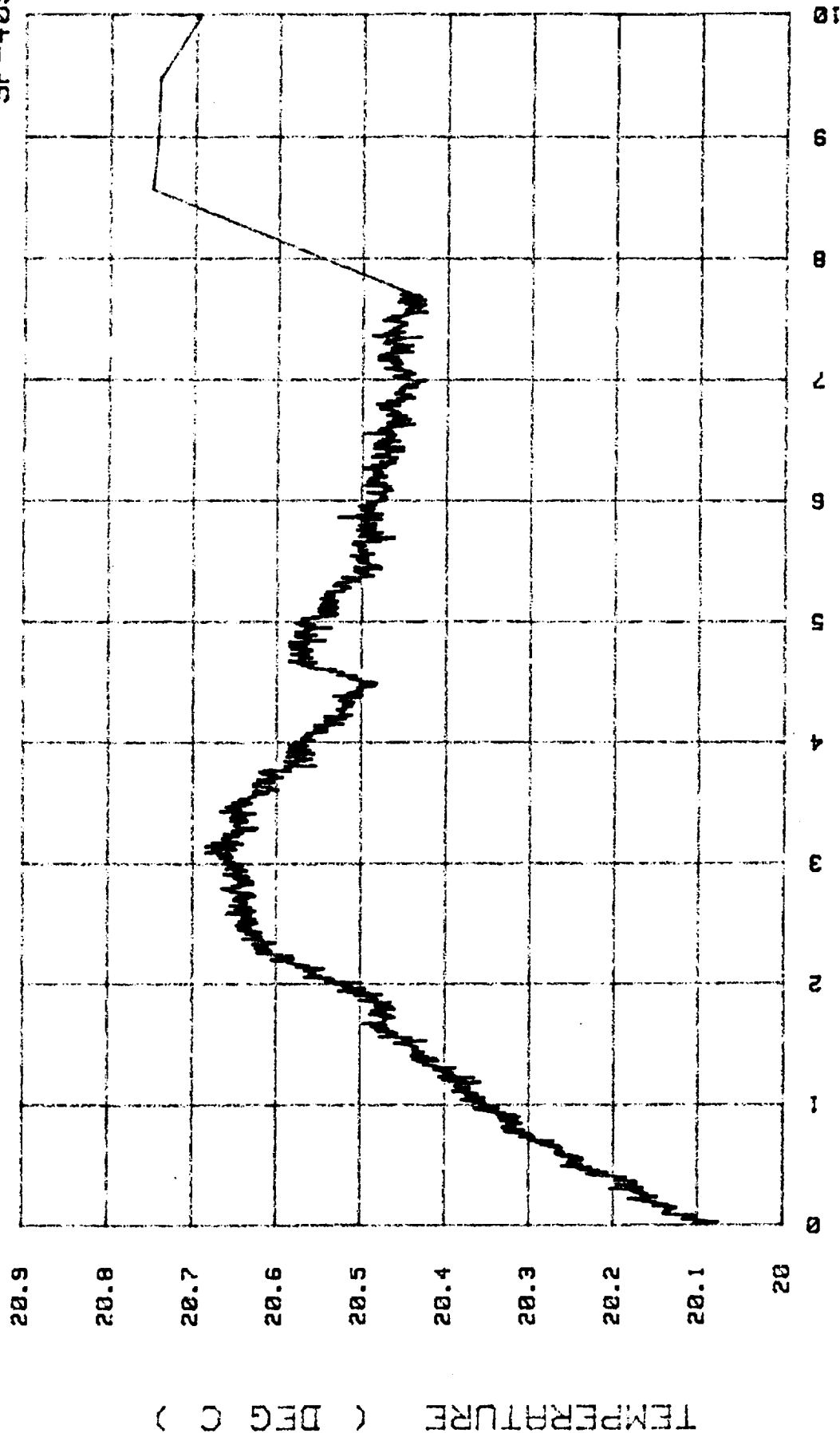


FIG. 15

Li/SOC12 CELL PREFORMANCE TEST

CELL #1

6 Dec 1995

SF-409

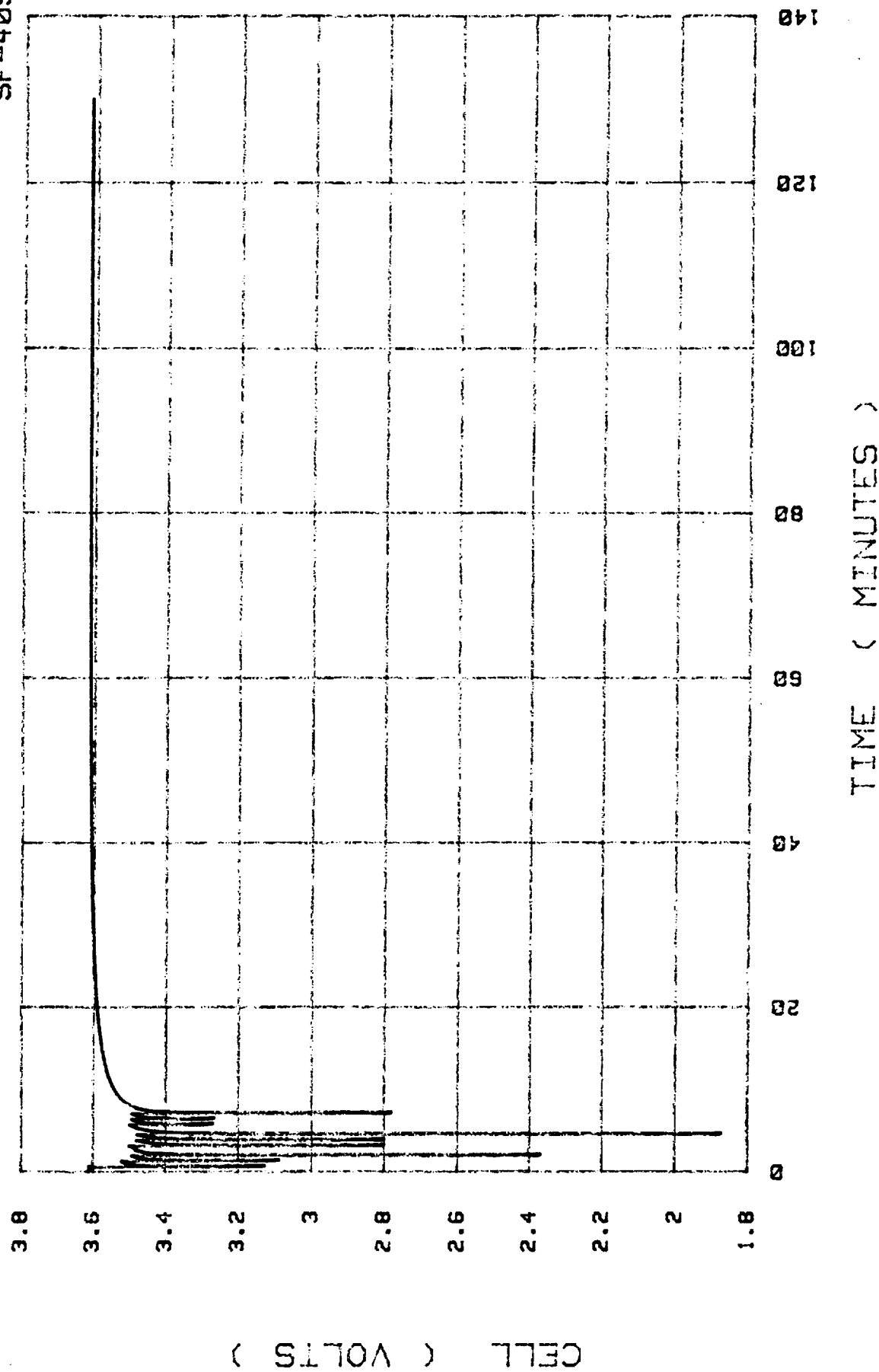
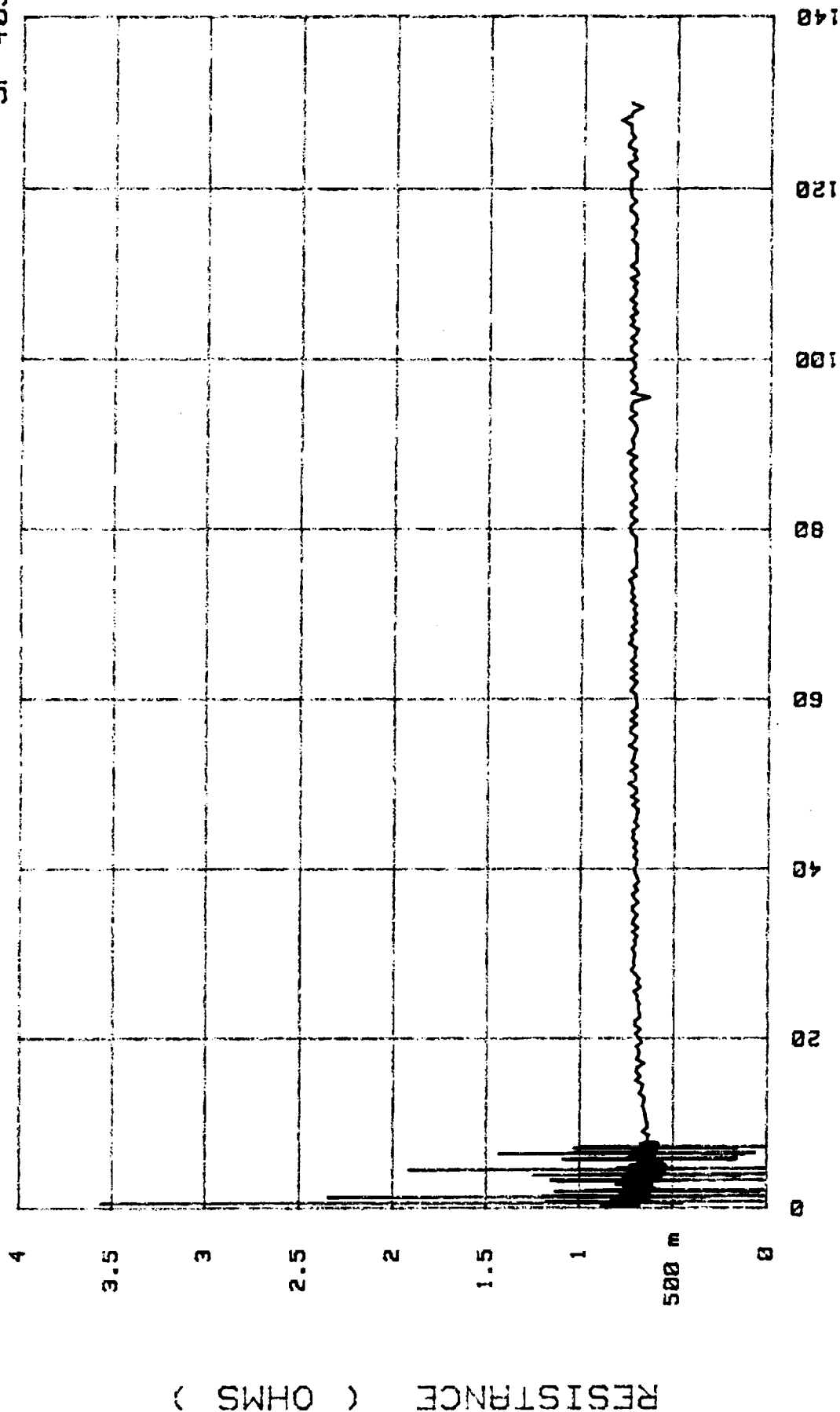


FIG. I6

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

6 Dec 1995
SF-409



CELL1_DCH_1: Channel 3

FIG J1

Li/SOC12 CELL PERFORMANCE TEST

+40°C
CELL #1
7 Dec 1995
SF-409

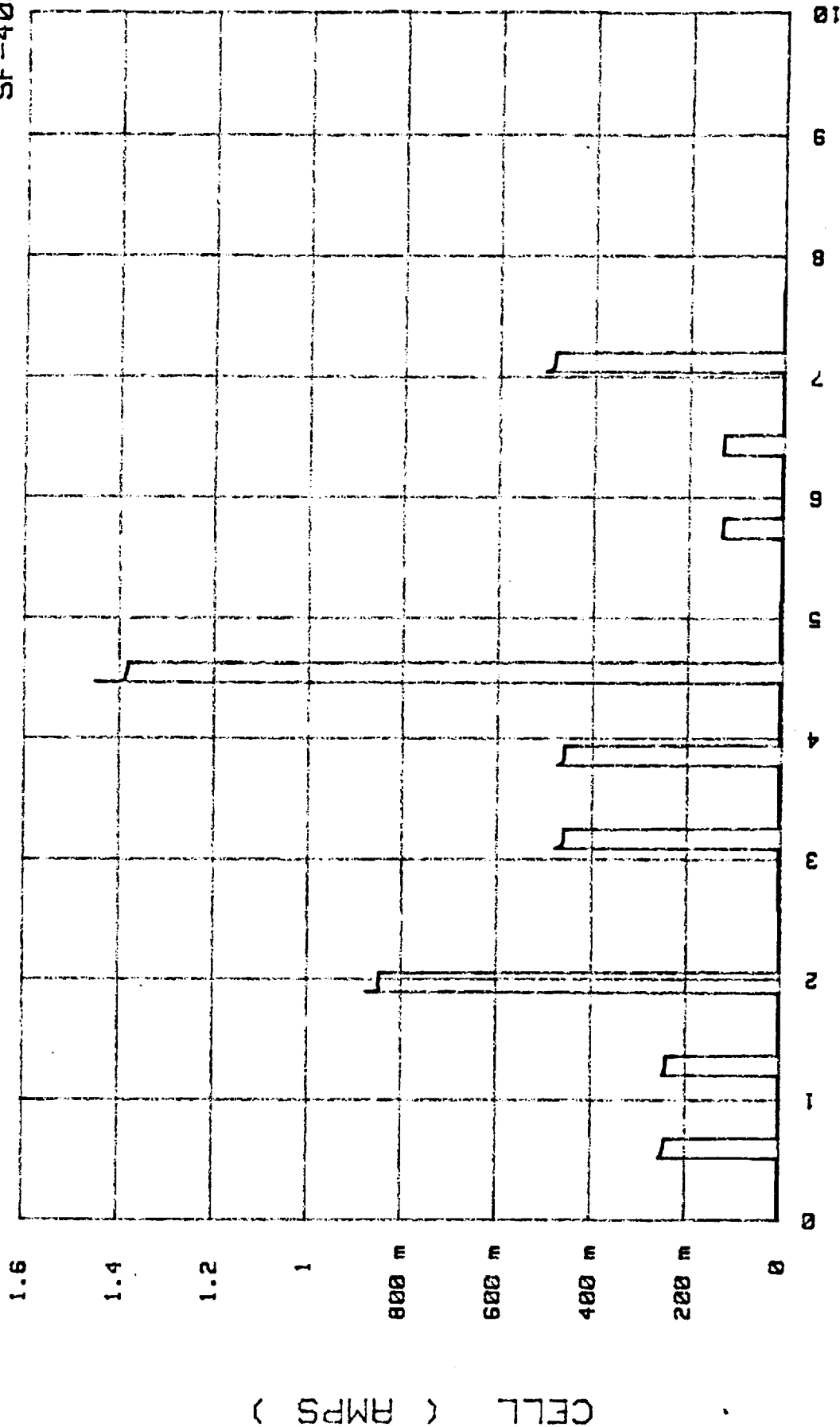


FIG. 52

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

7 Dec 1995
SF-409

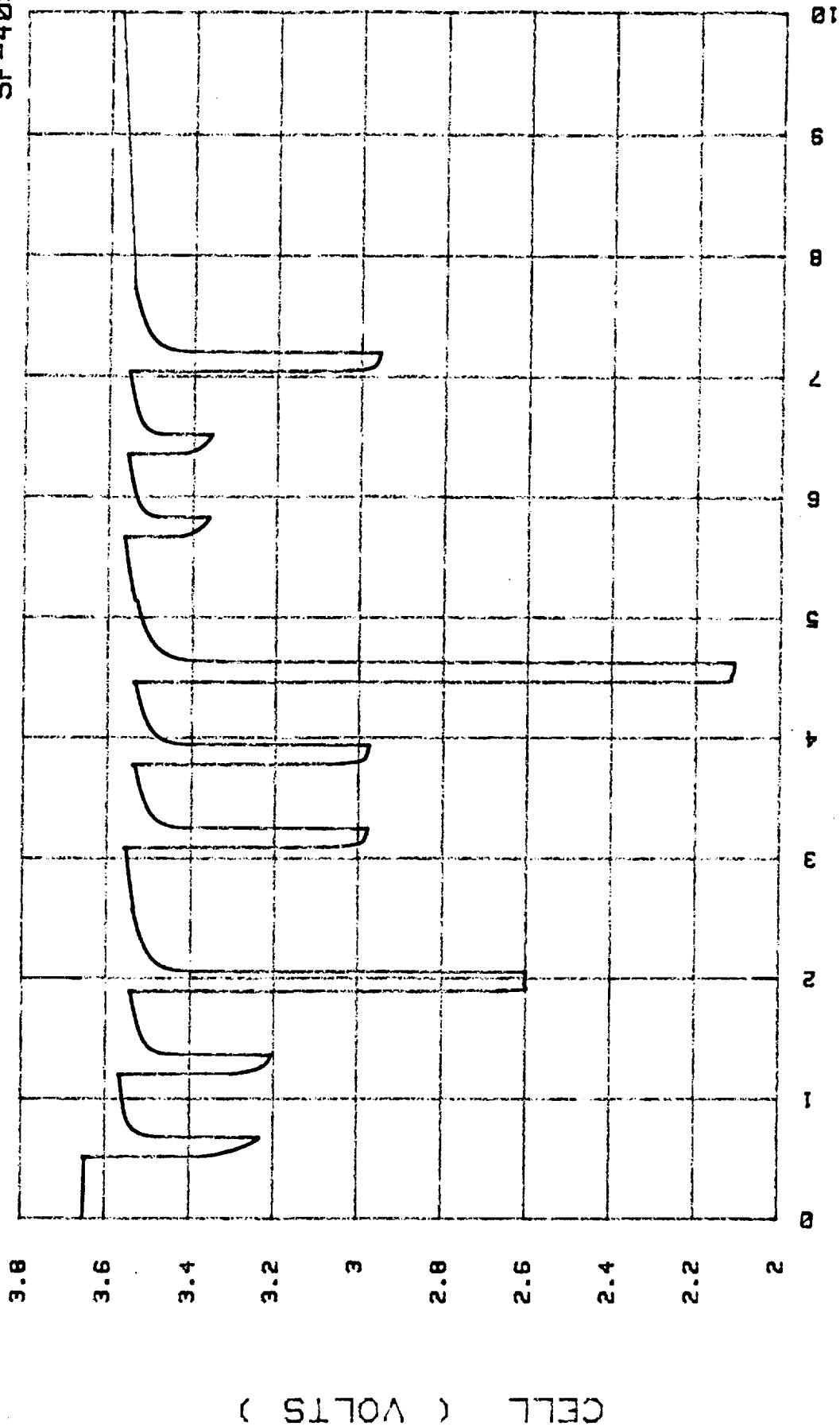


FIG. J3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

7 Dec 1995
SF-409

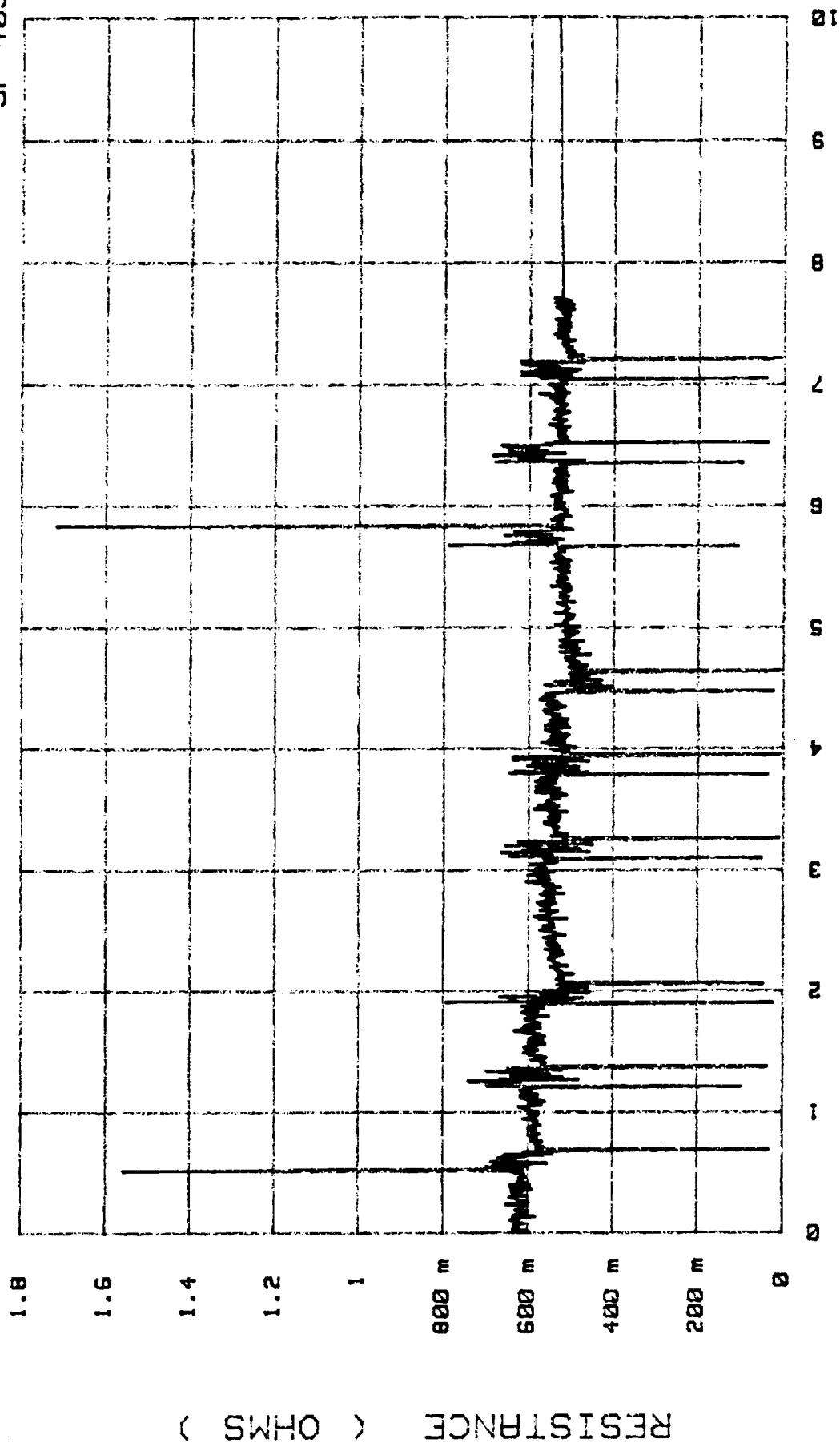


FIG. 54

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

7 Dec 1995
SF-409

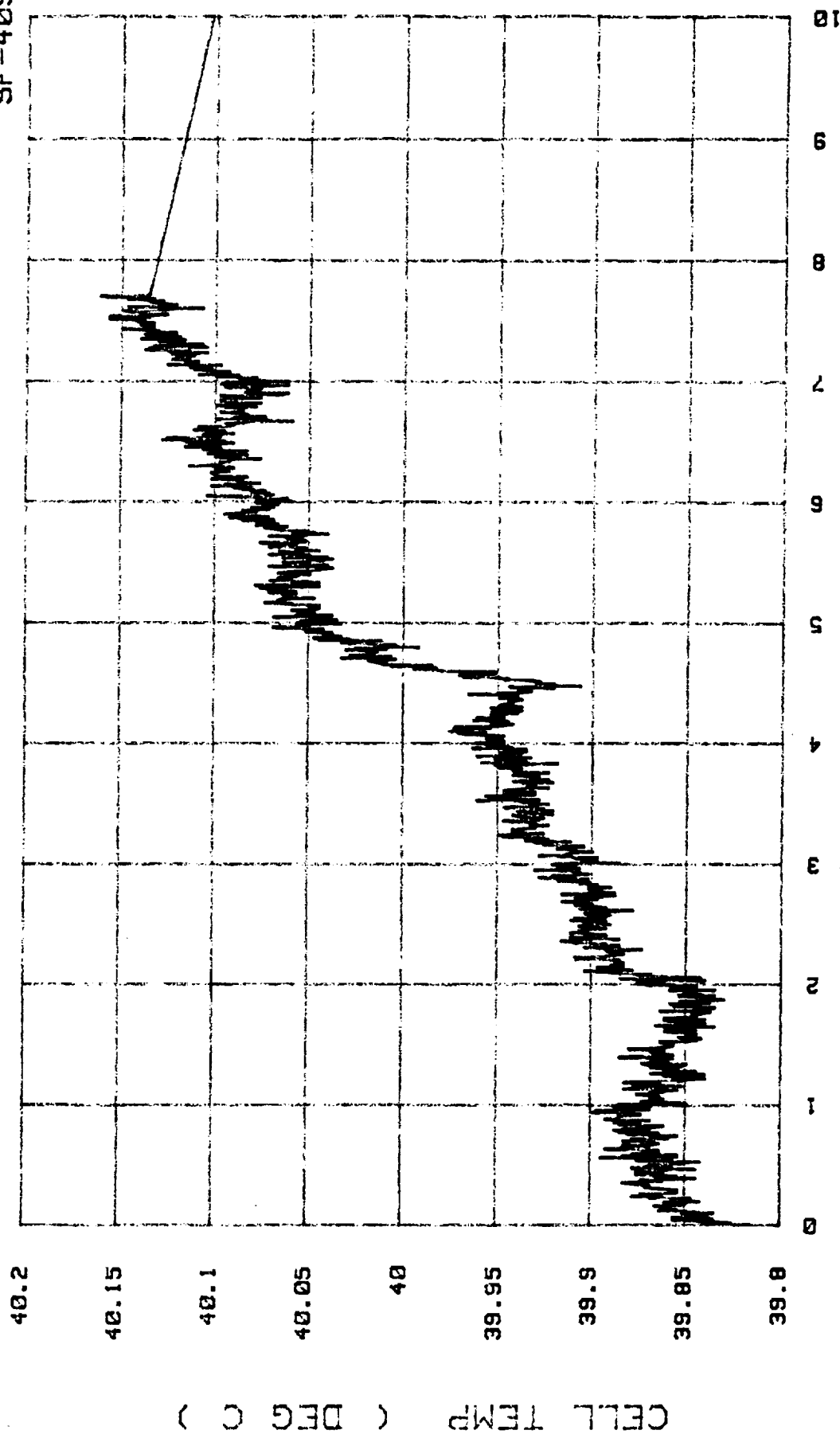


FIG. K1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

0°C (AFTER +40°C)

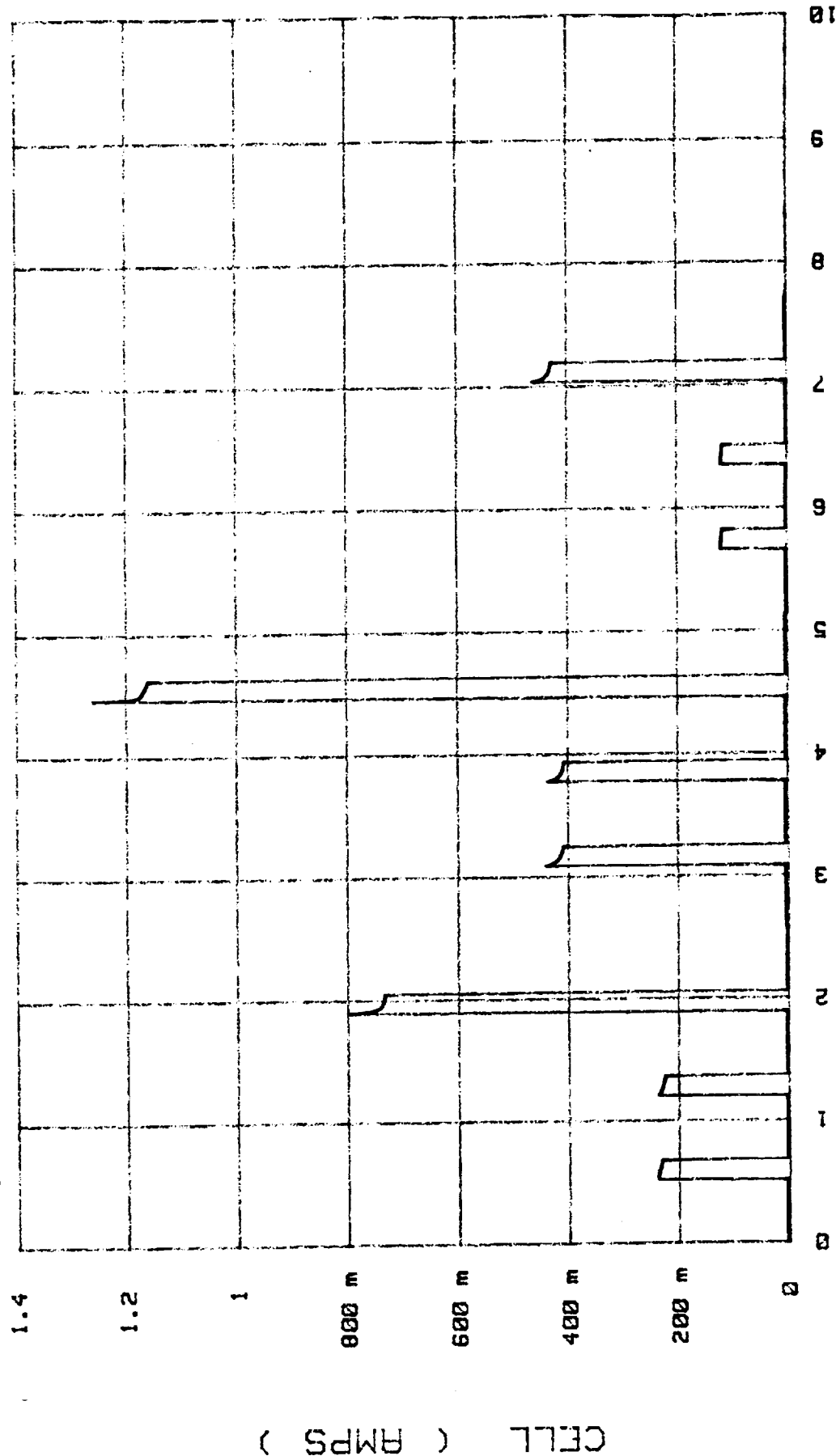


FIG. K2

LI/SOCI2 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

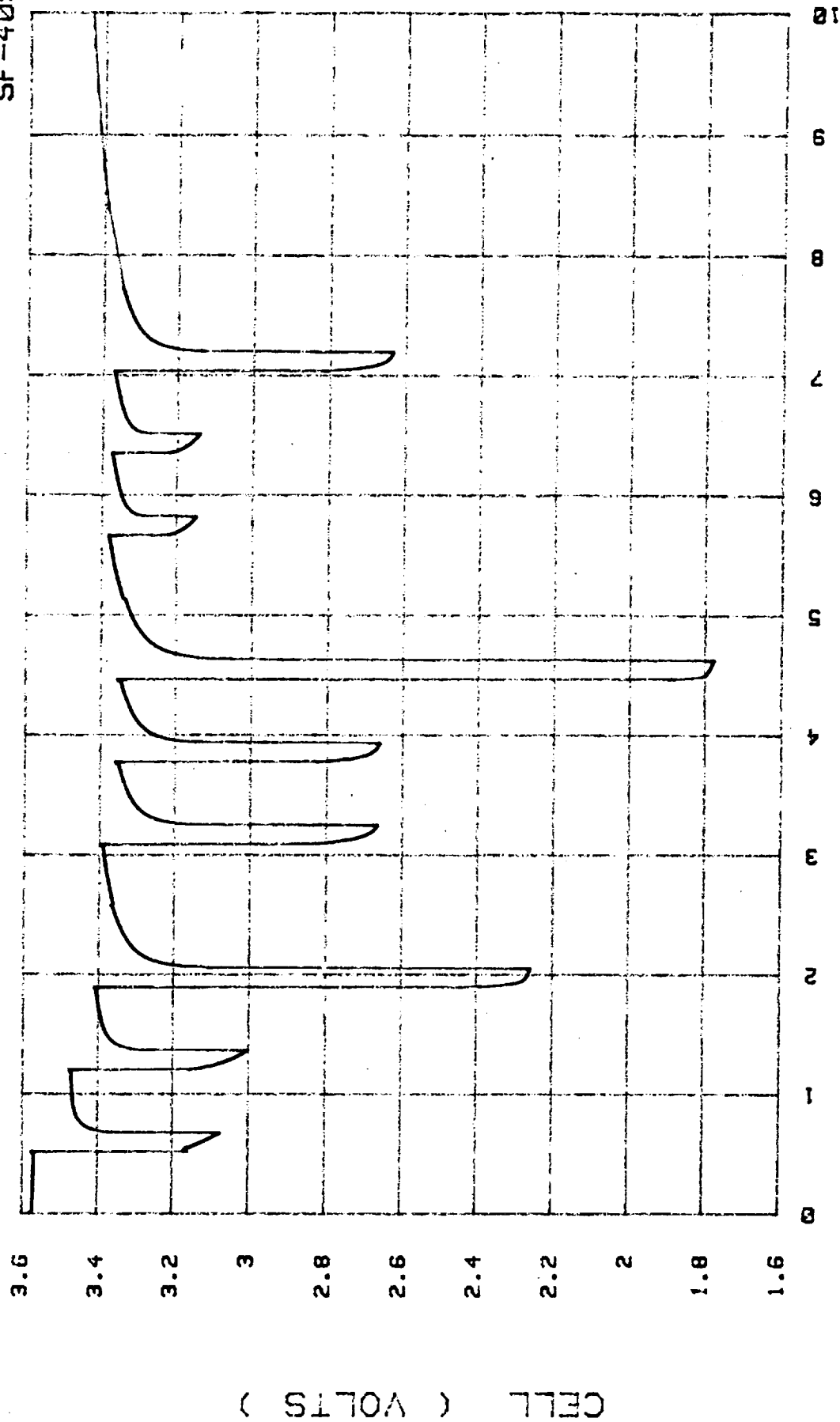


FIG. K3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995

SF-409

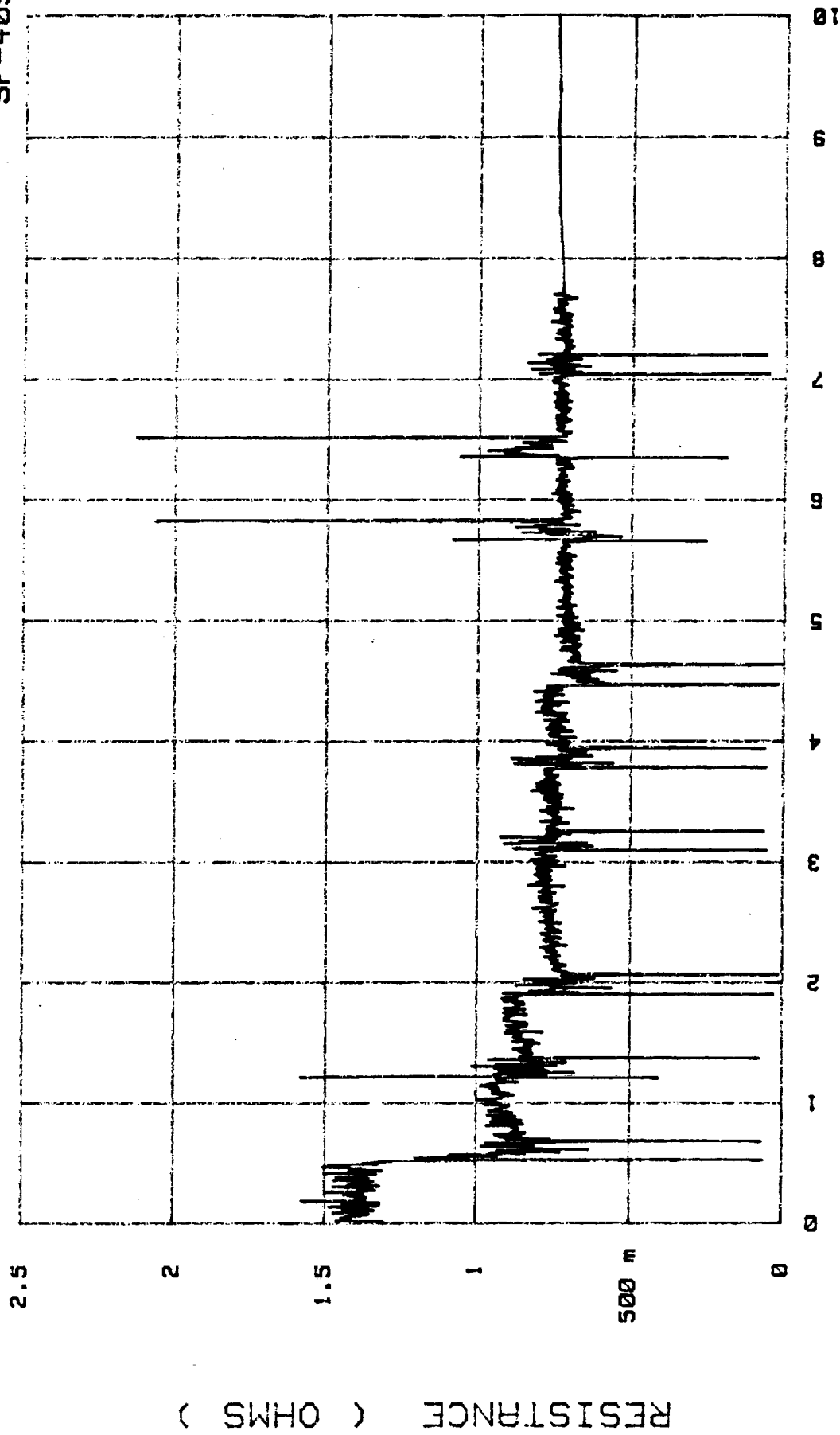


FIG. K4

Li/SOC12 CELL PREFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

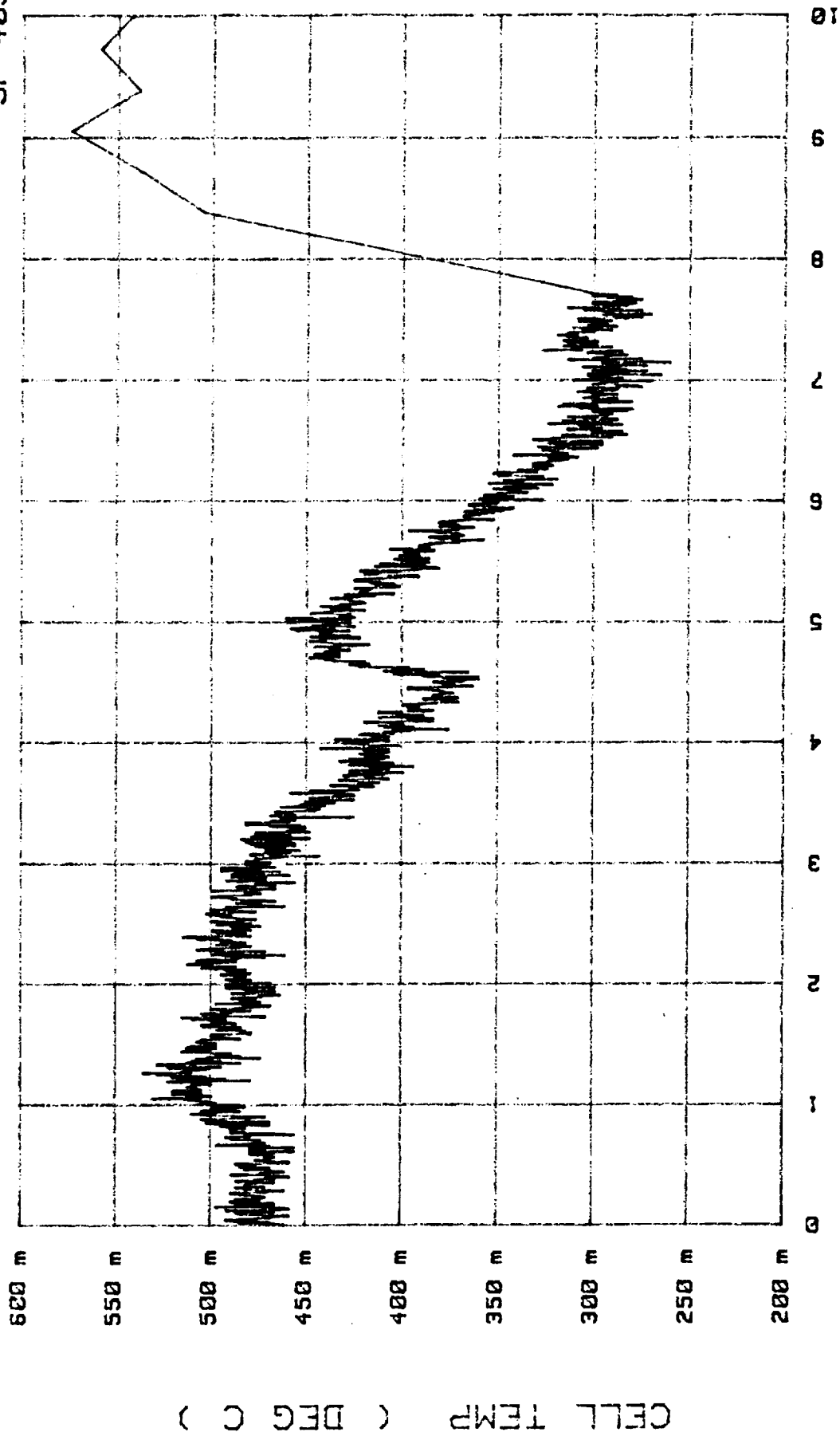


FIG. 1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

-65°C

8 Dec 1995
SF-409

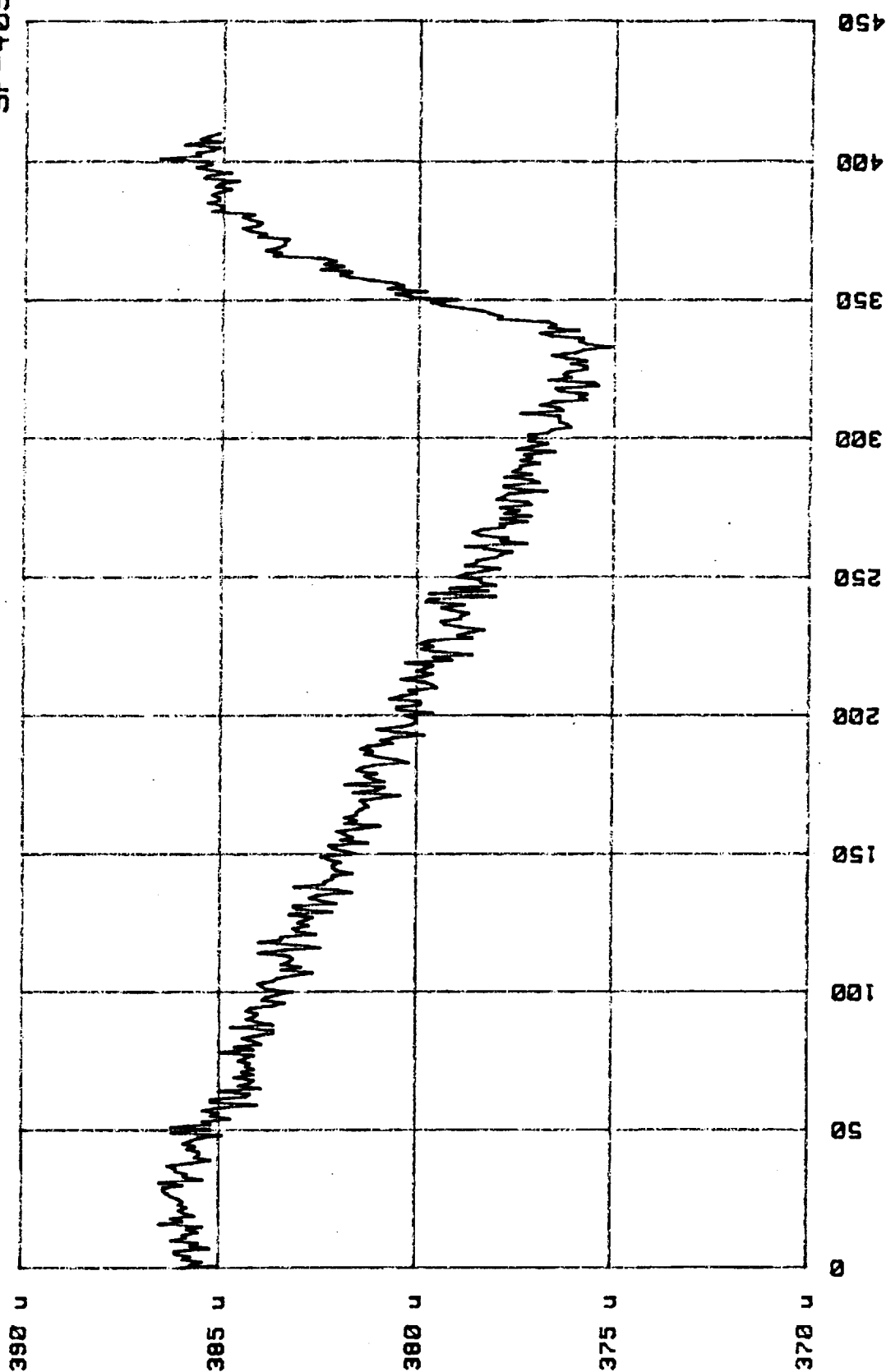


FIG. 2

Li/SOCI2 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

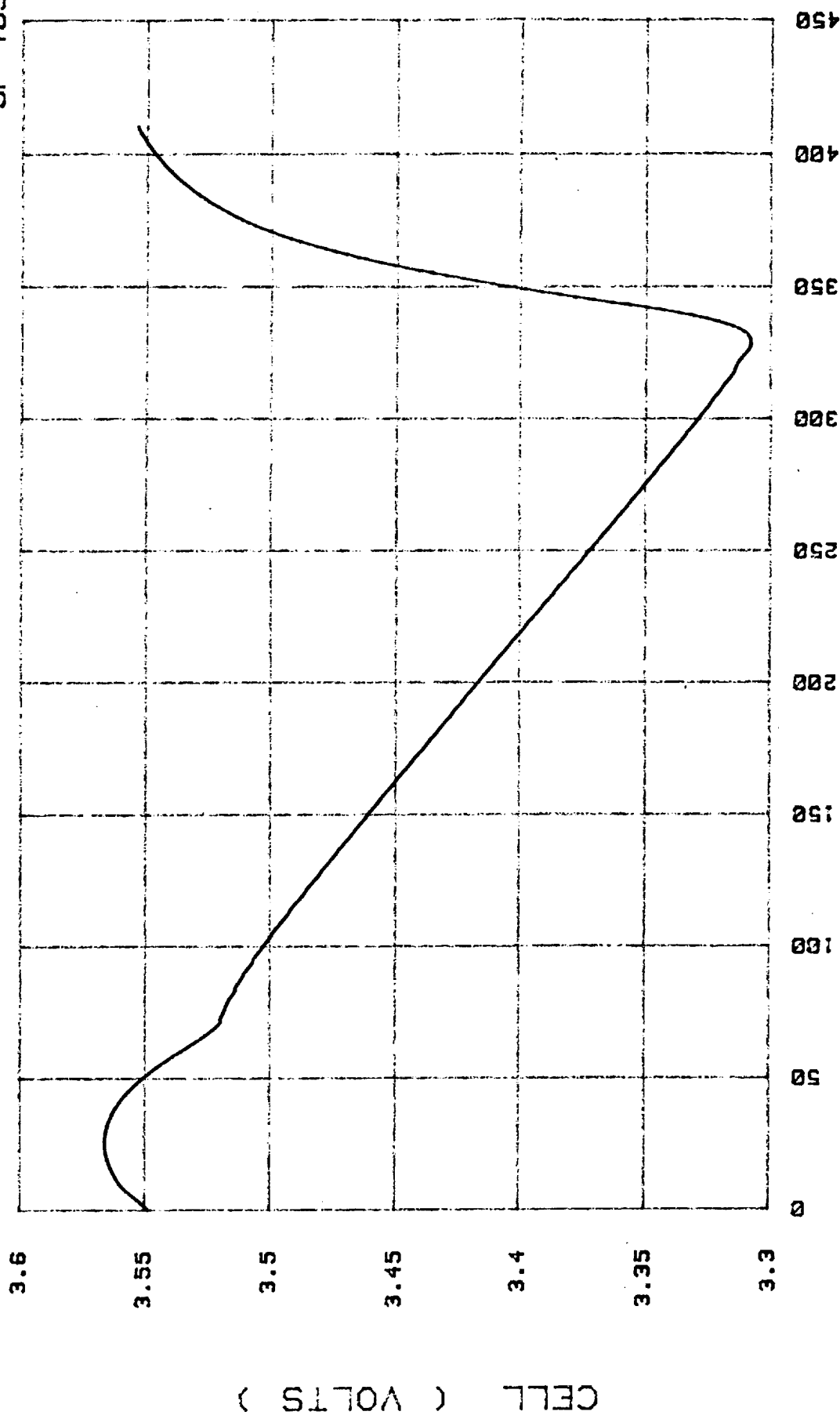


FIG. L3

Li/SOC12 CELL PREFORMANCE TEST

CELL #1

8 Dec 1995

SF-409

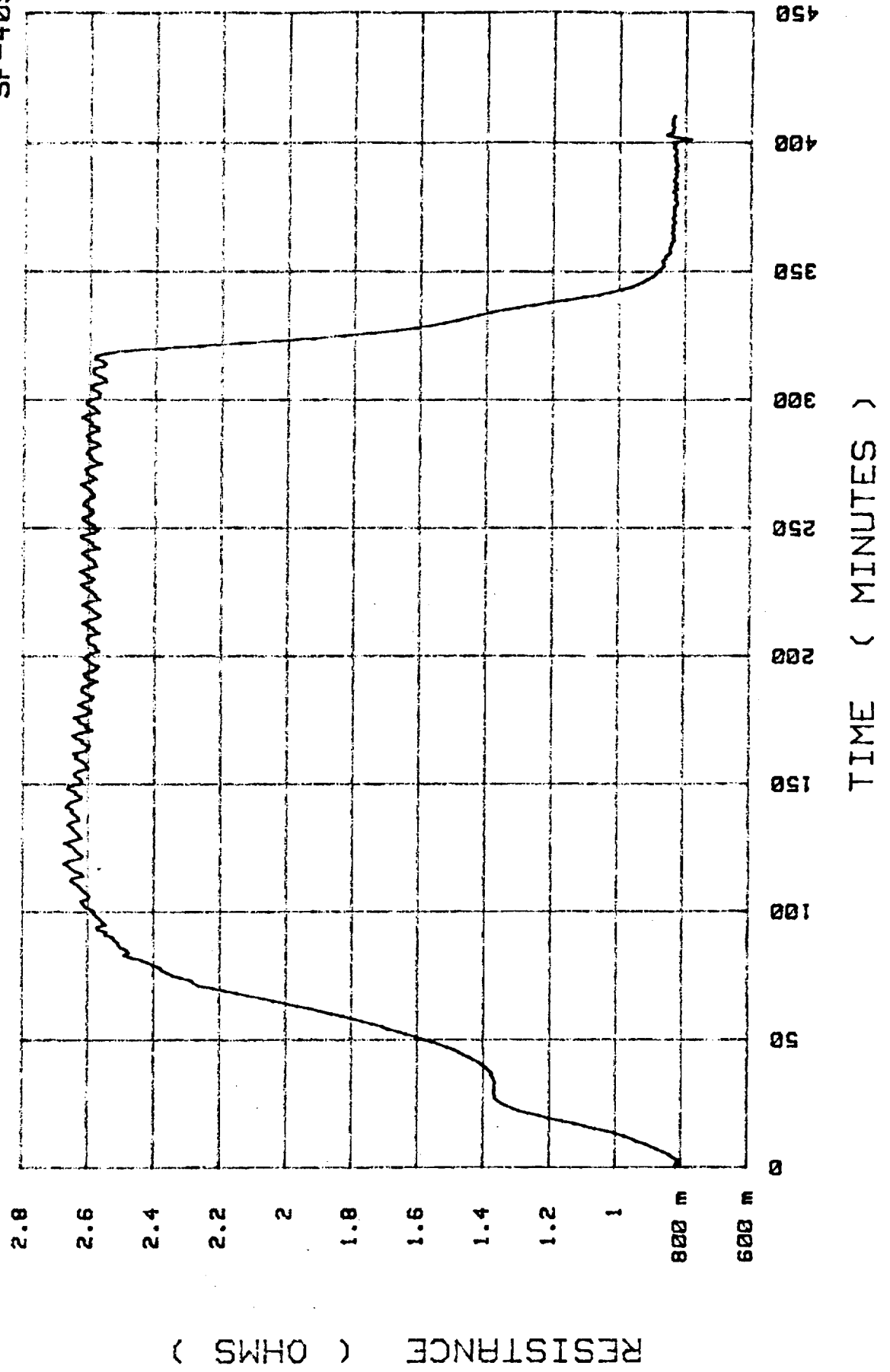


FIG. 44

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

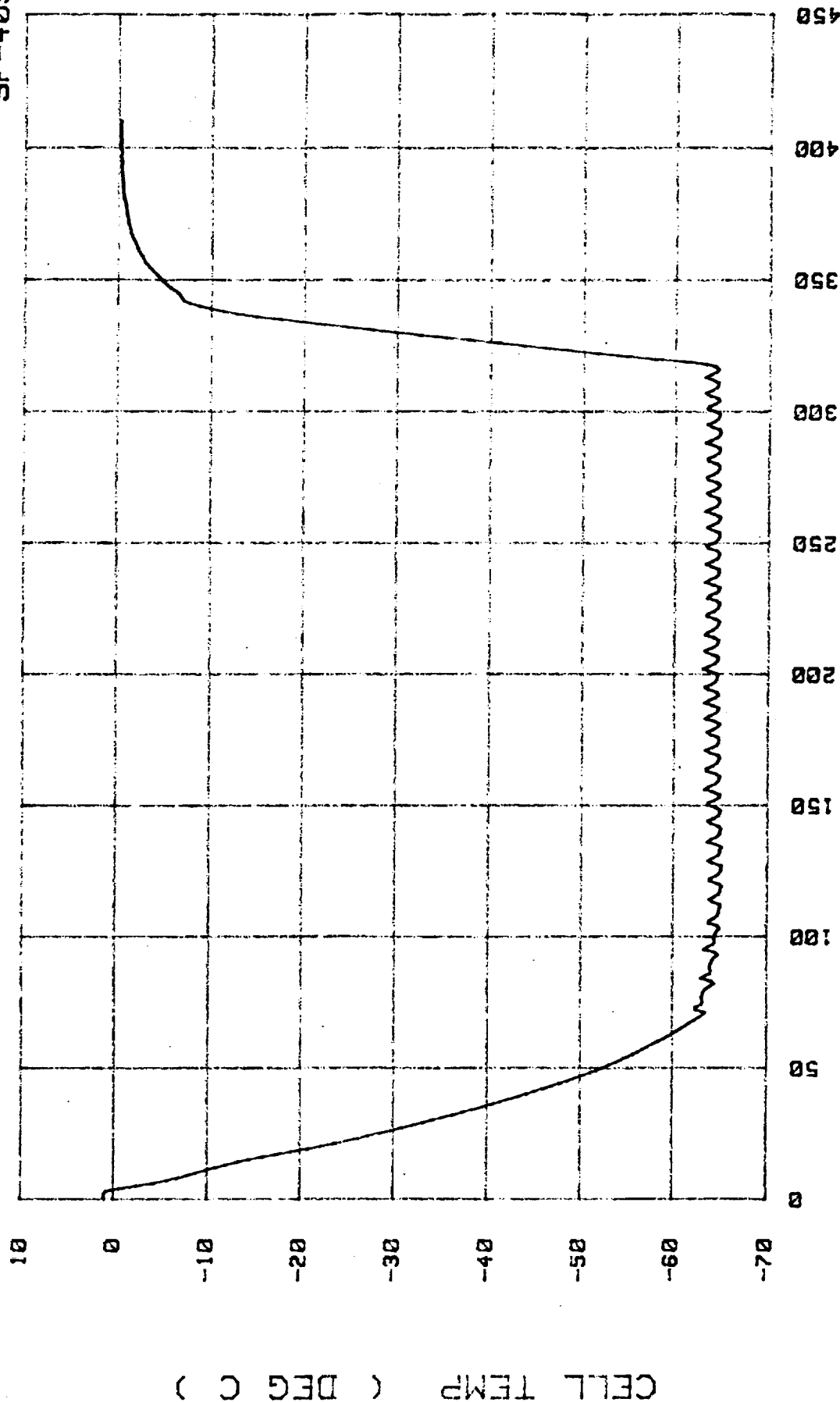
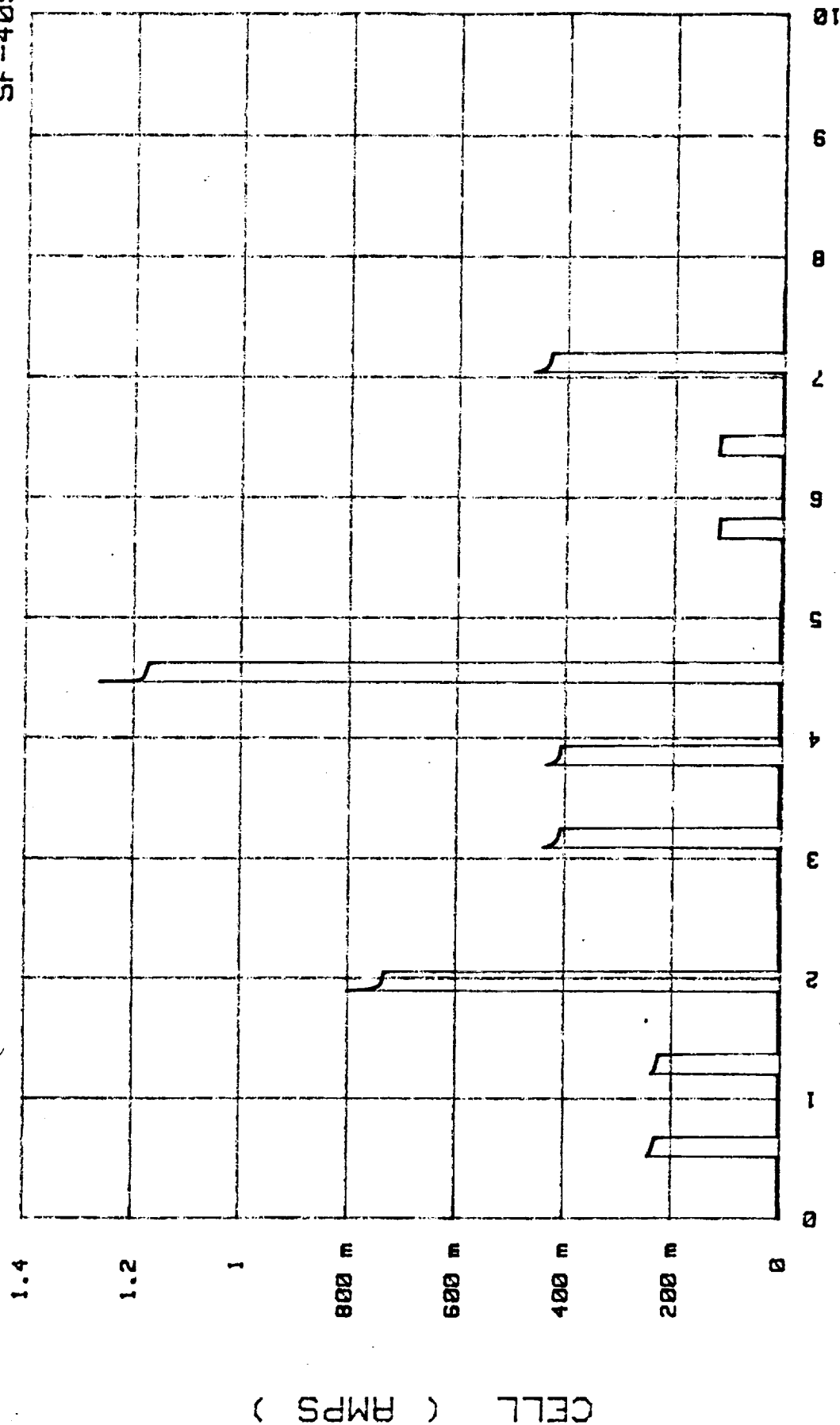


FIG. M1

Li/SOC12 CELL PERFORMANCE TEST

0°C (APPROX -65°C) CELL #1

8 Dec 1995
SF-409



TIME (MINUTES)

CELL1_DCH_M: Channel 1

FIG. M2.

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

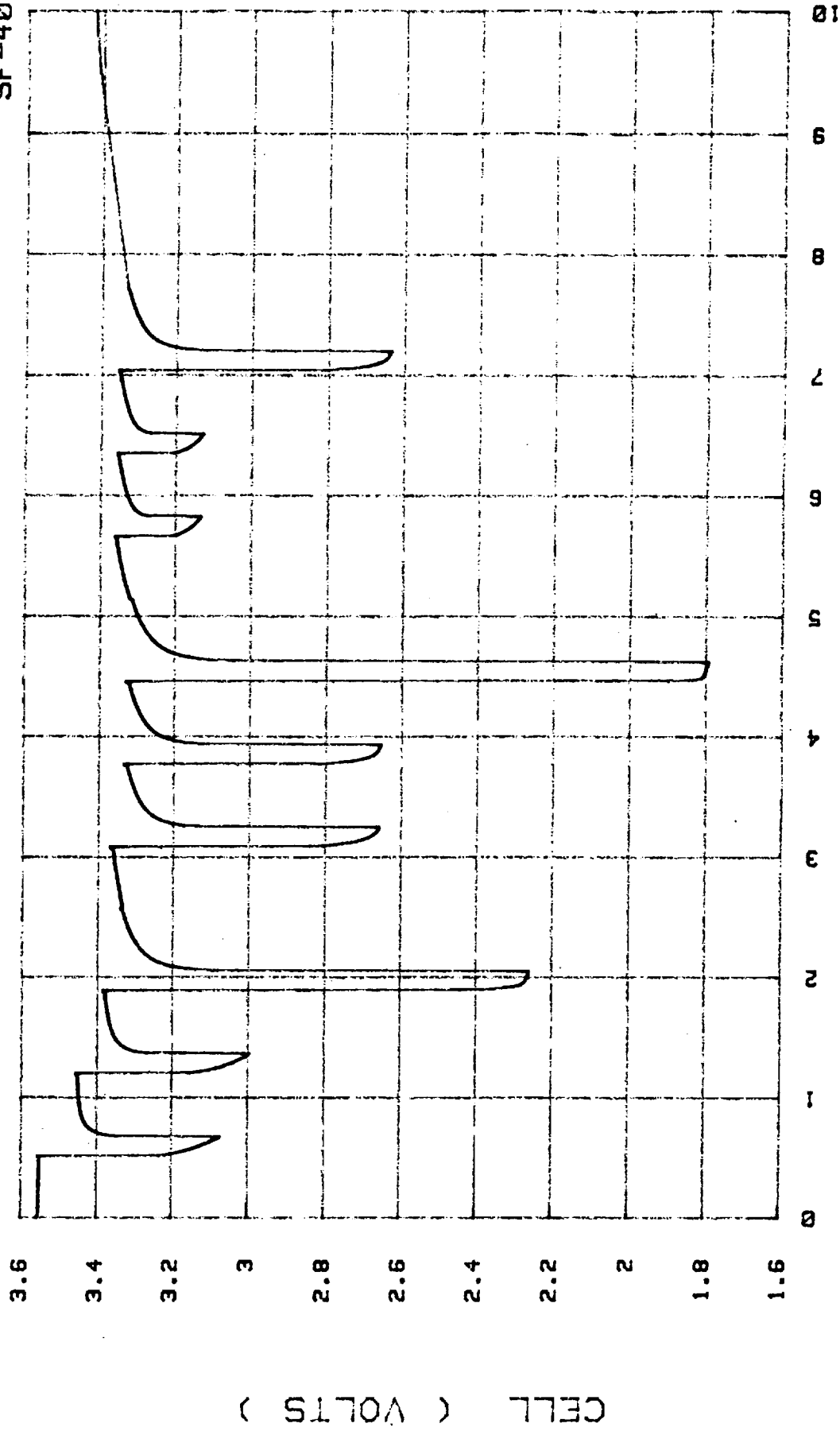


FIG. M3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

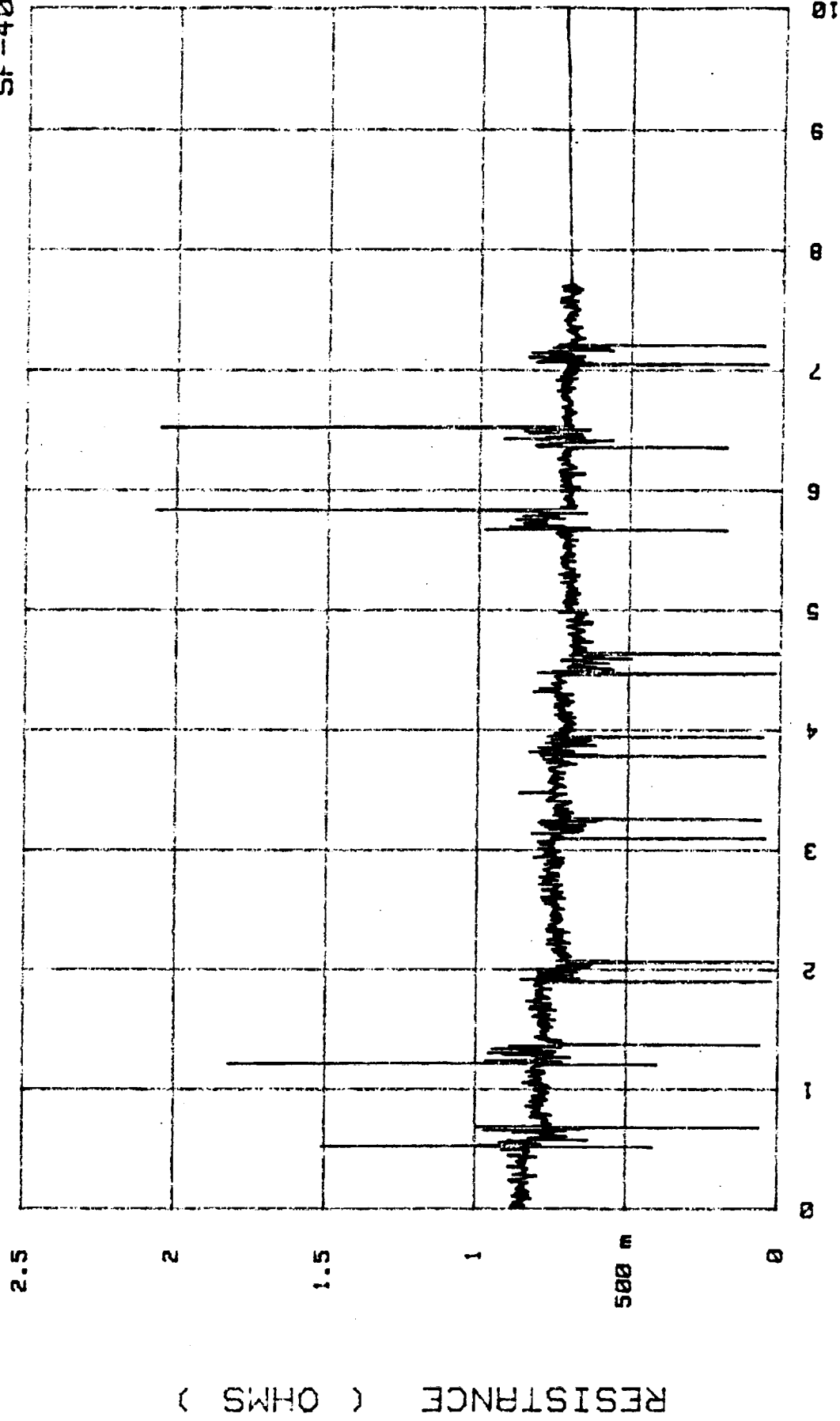


FIG. M4

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

8 Dec 1995
SF-409

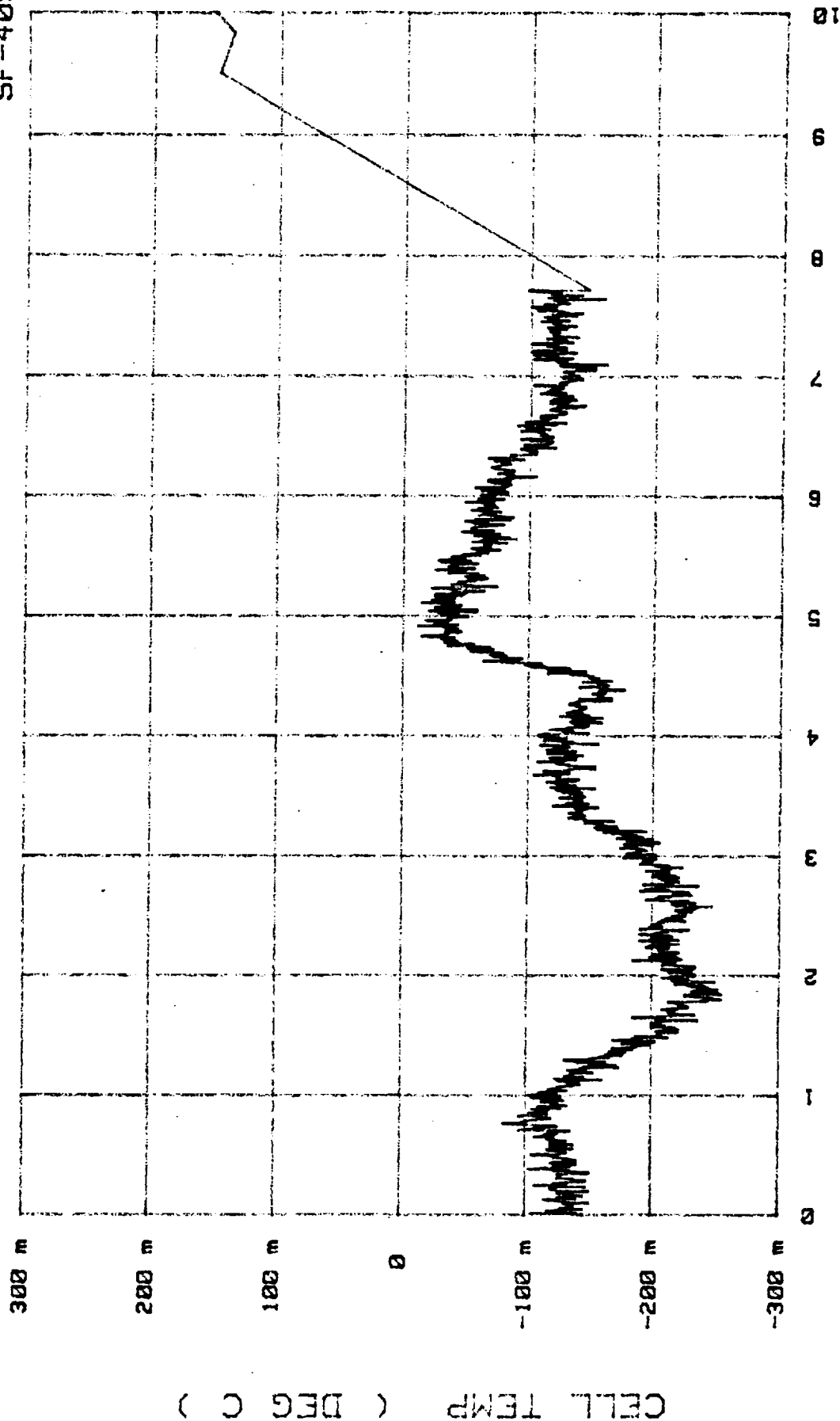


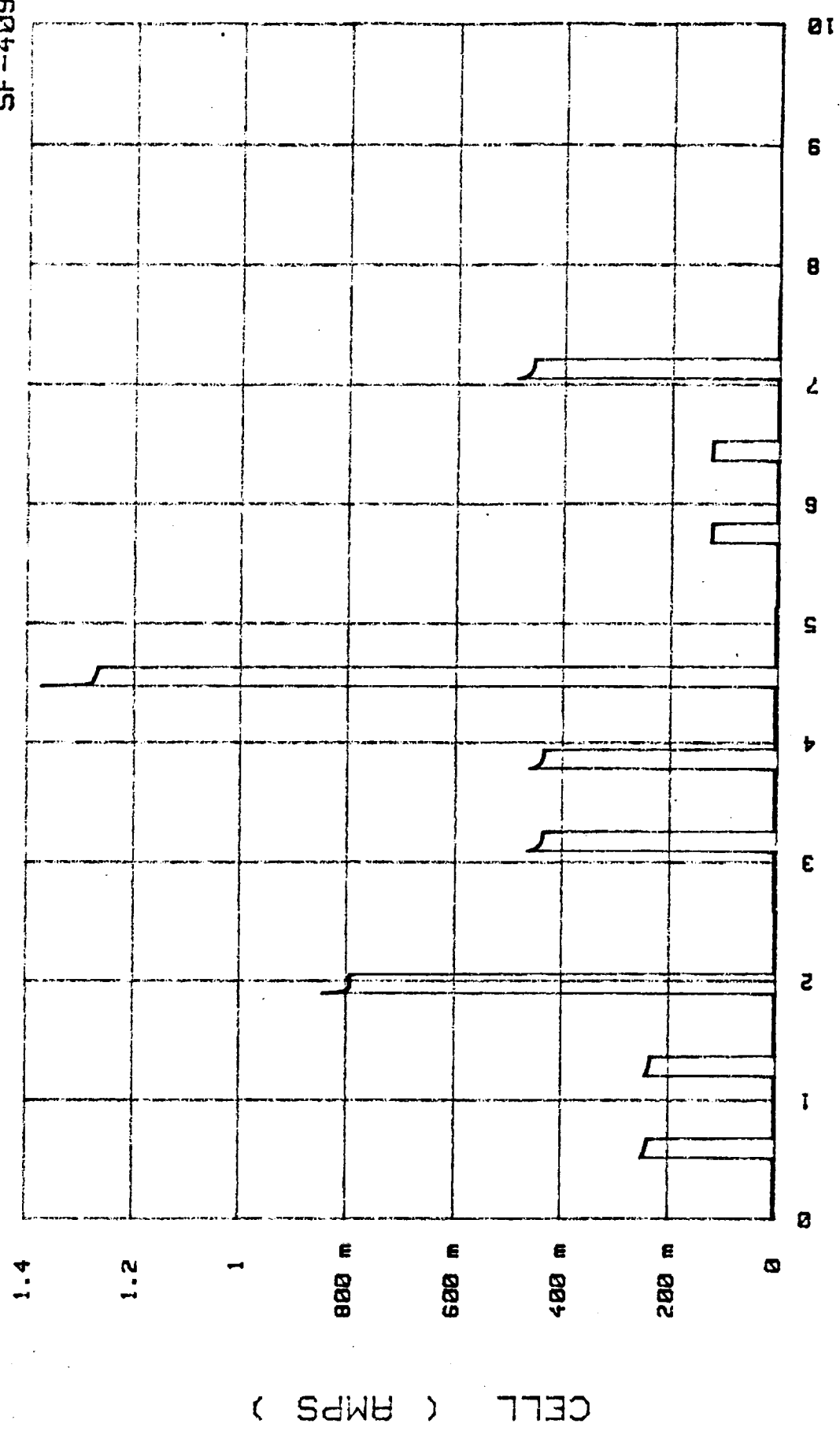
FIG. A1

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

+20°C

11 Dec 1995
SF-409



TIME (MINUTES)

CELL1_DCH_N: Channel 1

FIG. N2

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

11 Dec 1995

SF-409

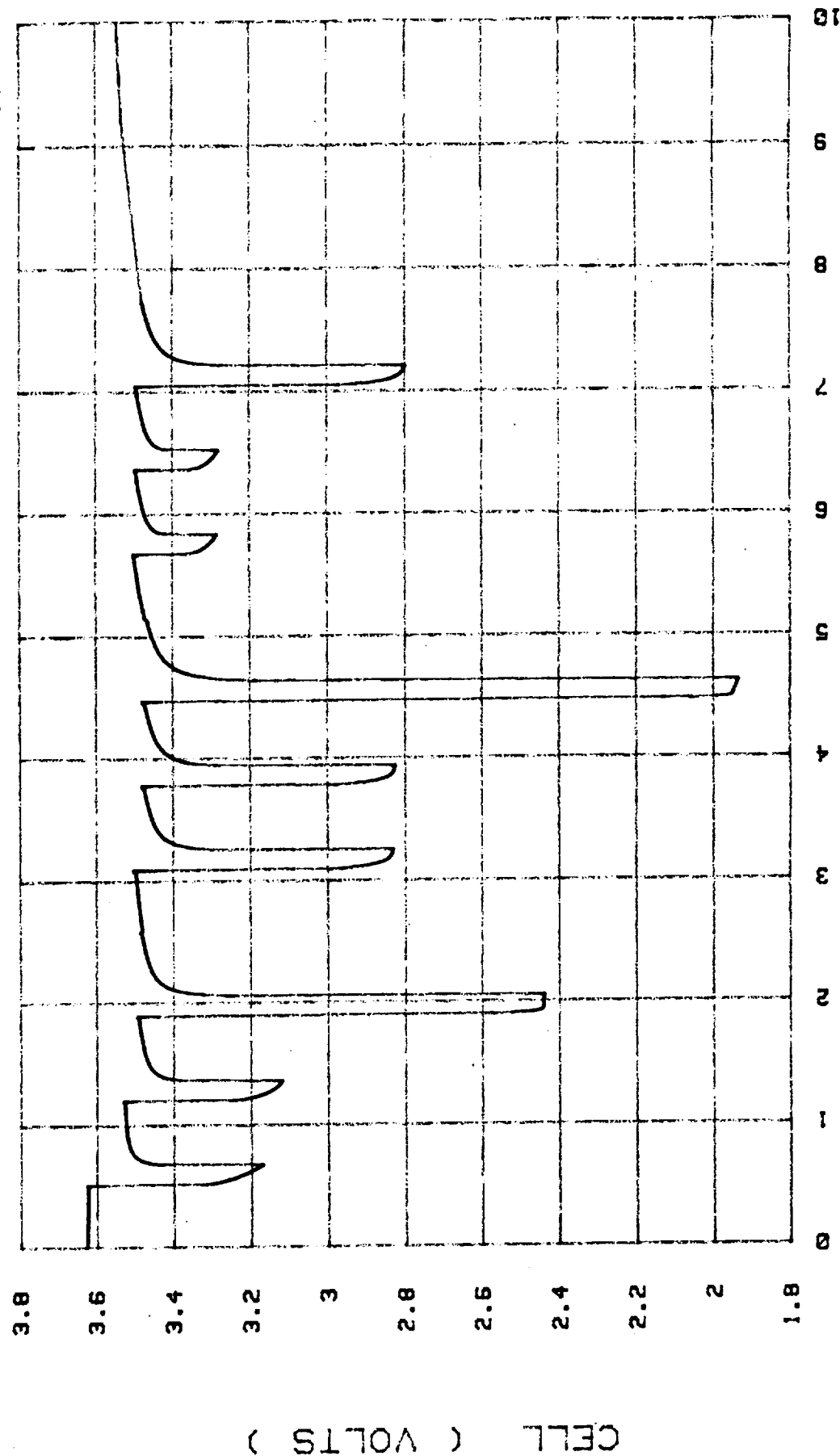


FIG. N3.

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

11 Dec 1995
SF-409

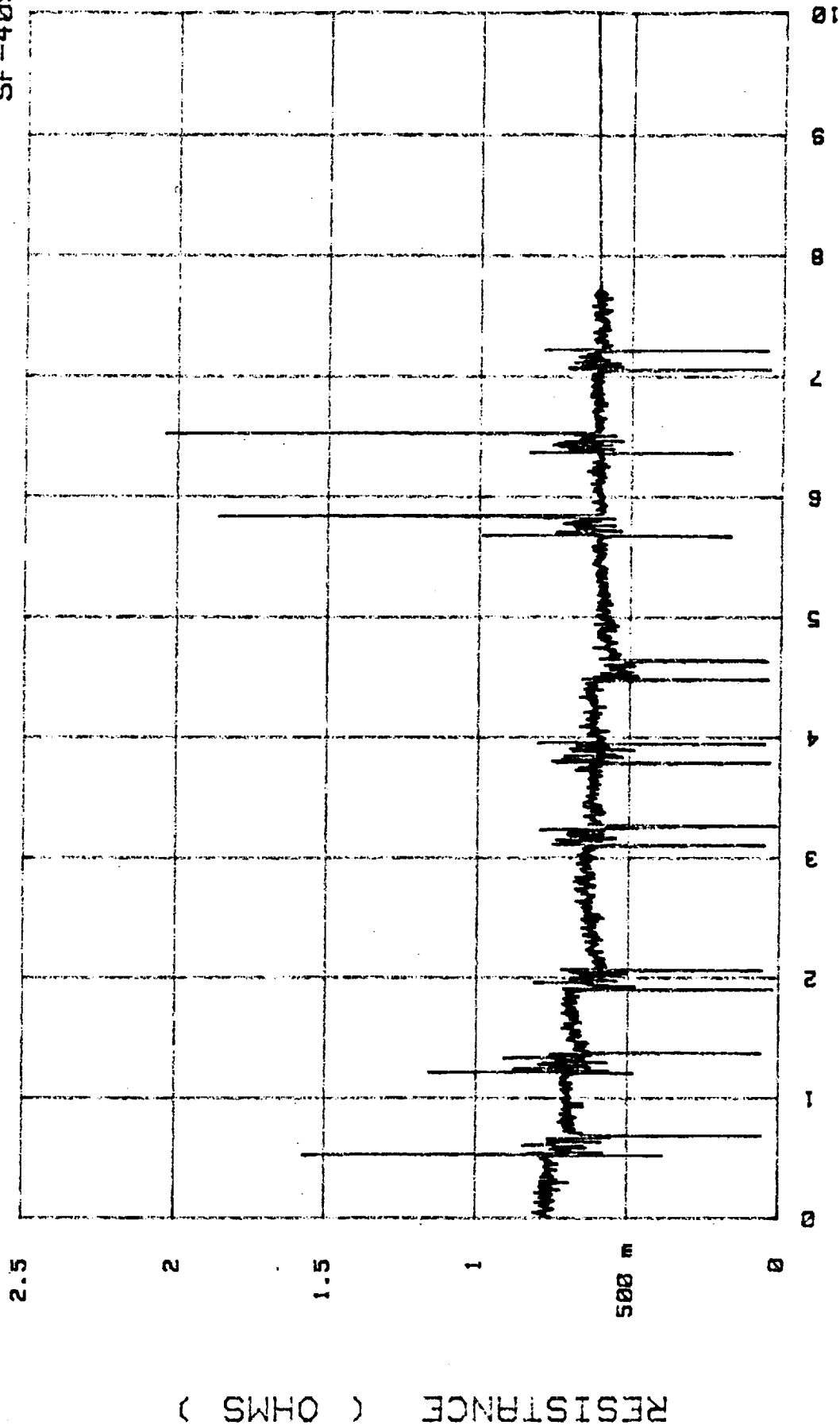


FIG. N4

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

11 Dec 1995
SF-409

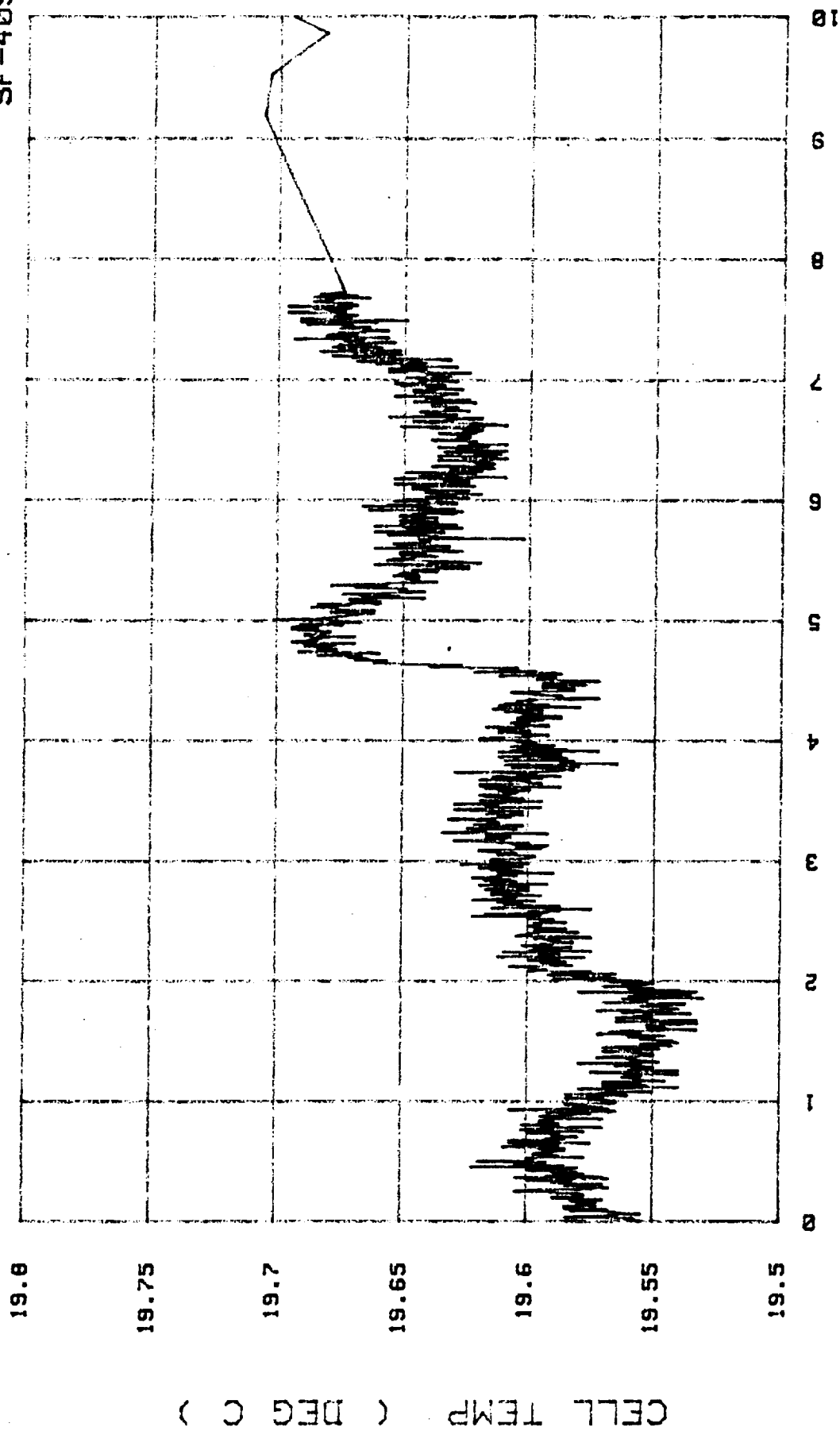


FIG. 01

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

12 Dec 1995
SF-409

+60°C

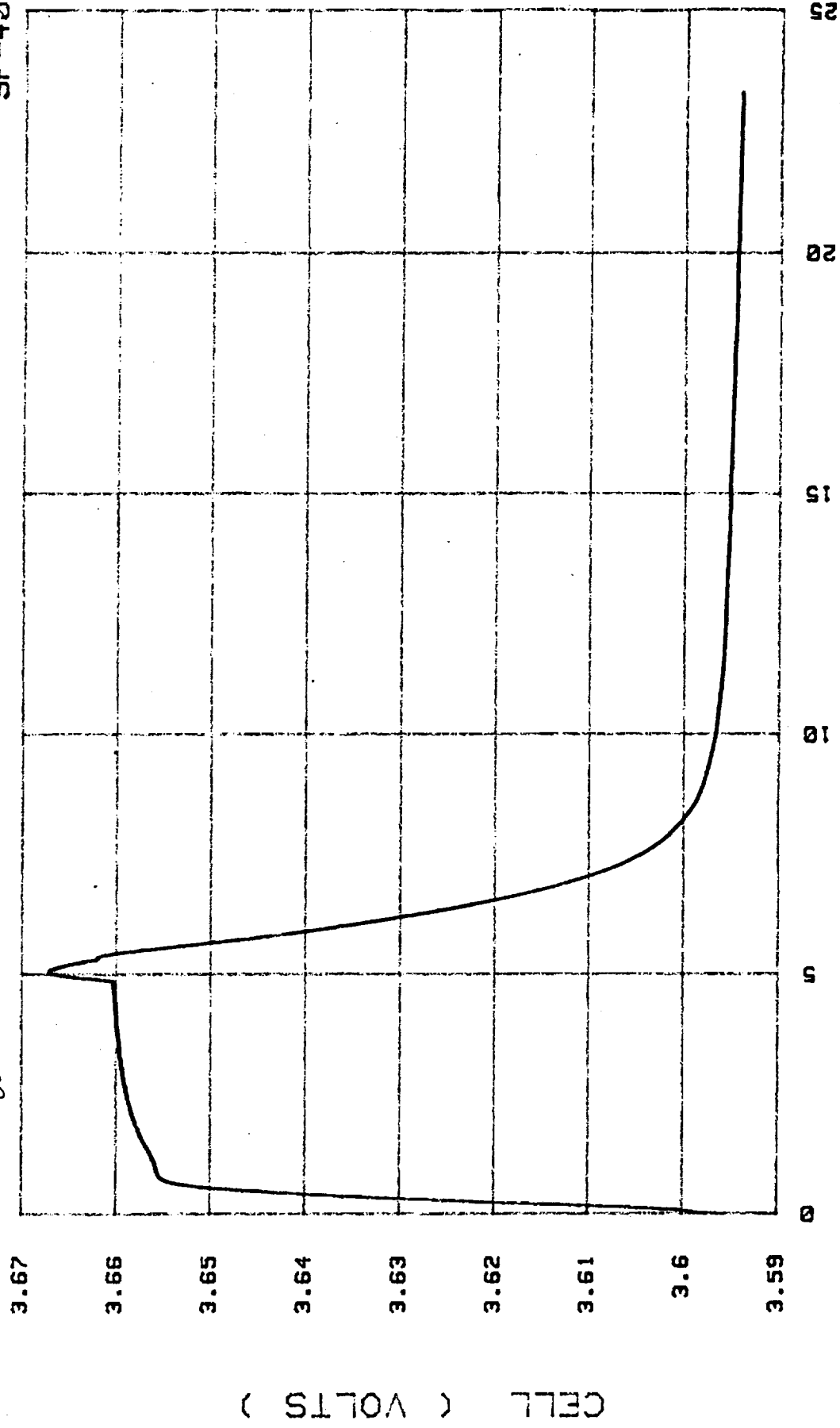


FIG. 02

Li/SOCI2 CELL PREFORMANCE TEST

CELL #1

12 Dec 1995
SF-409

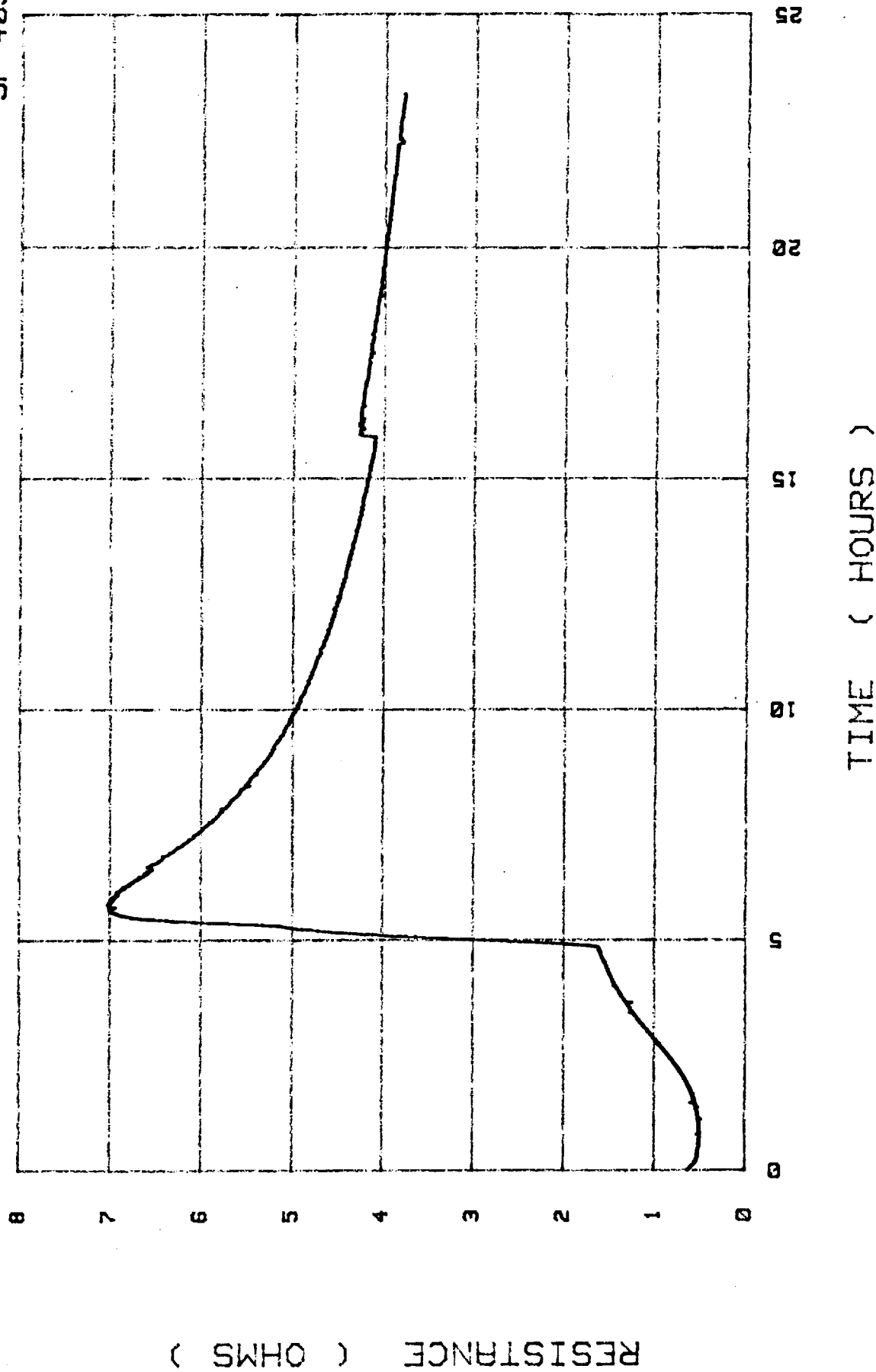


FIG. 03

Li/SOCI2 CELL PERFORMANCE TEST

CELL #1

12 Dec 1995
SF-409

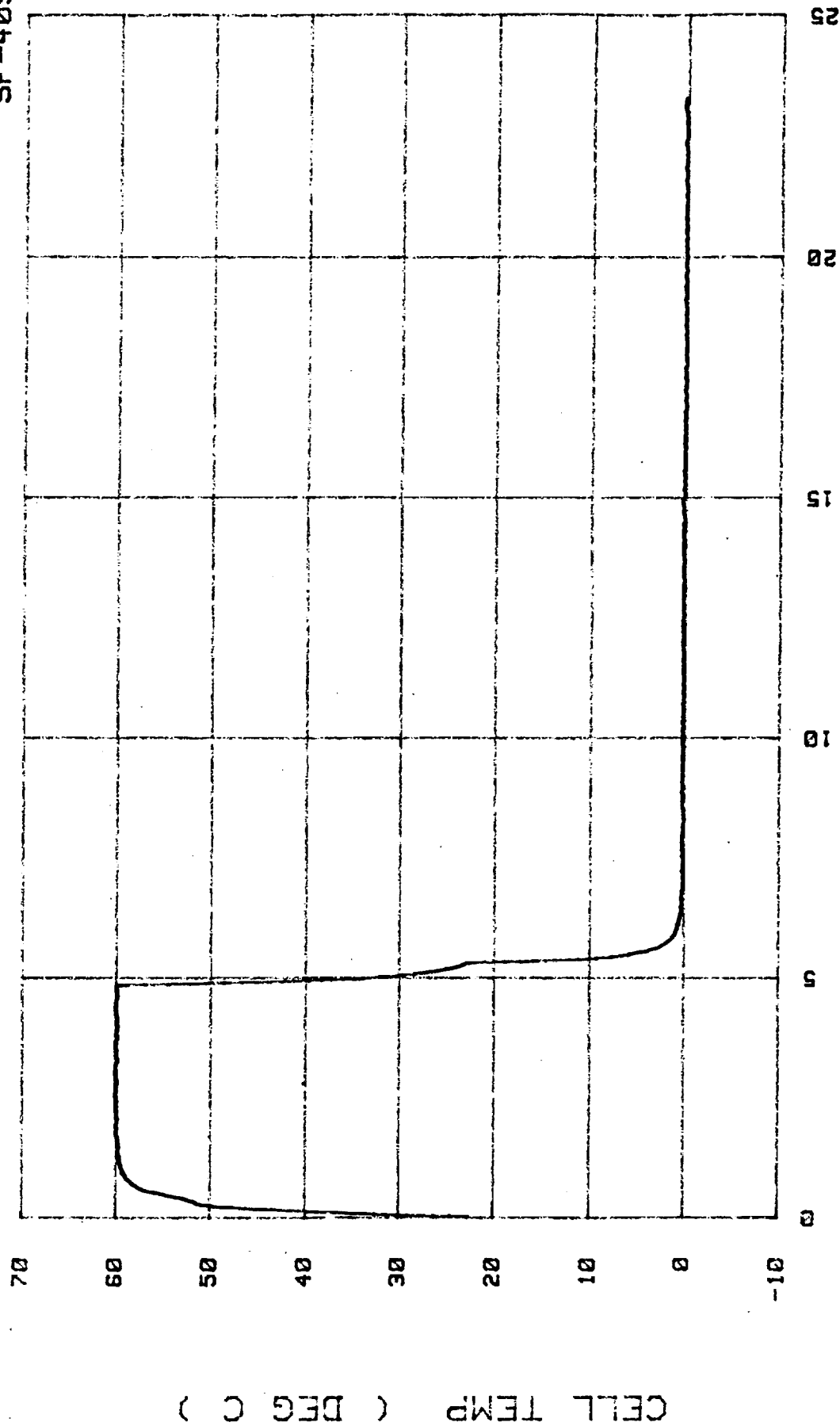


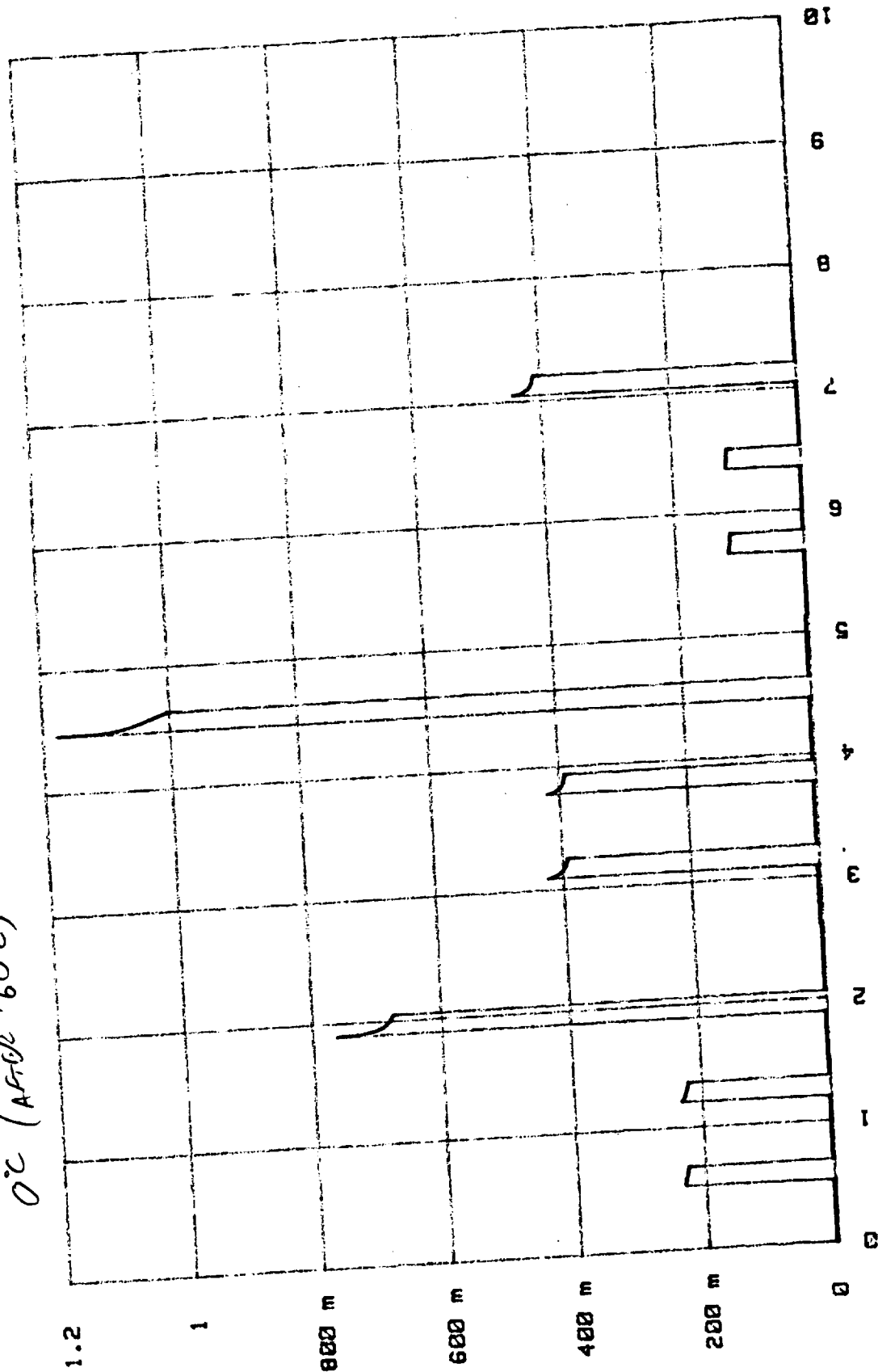
FIG. P1

Li/SOC12 CELL PREFORMANCE TEST

12 Dec 1995
SF-409

CELL #1

0°C (AFR + 60°C)



TIME (MINUTES)

CELL (RMPS)

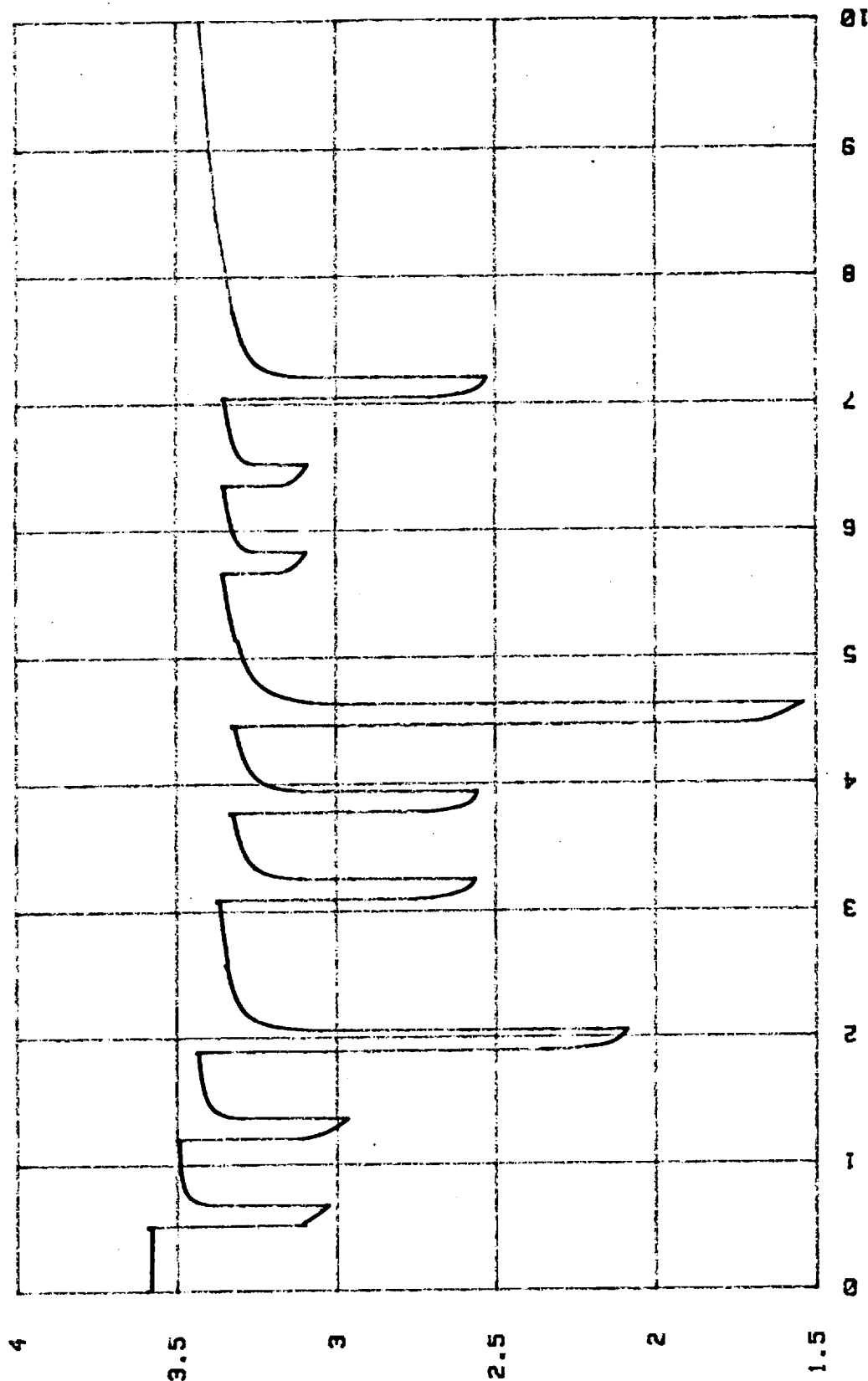
F16. P2

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

12 Dec 1995

SF-409



TIME (MINUTES)

CELL1_DCH_P: Channel 2

FIG. P3

Li/SOC12 CELL PERFORMANCE TEST

CELL #1

12 Dec 1995
SF-409

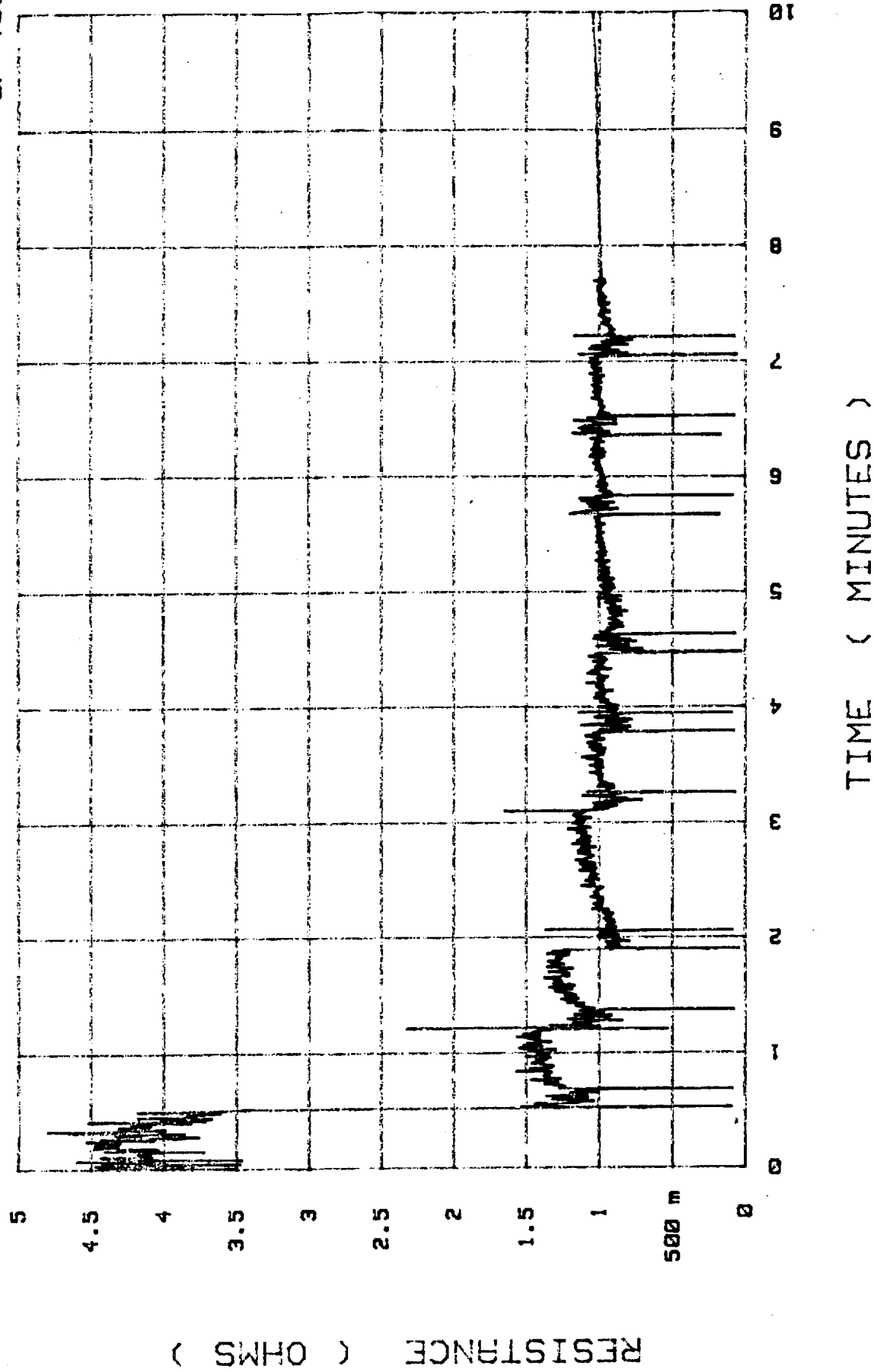
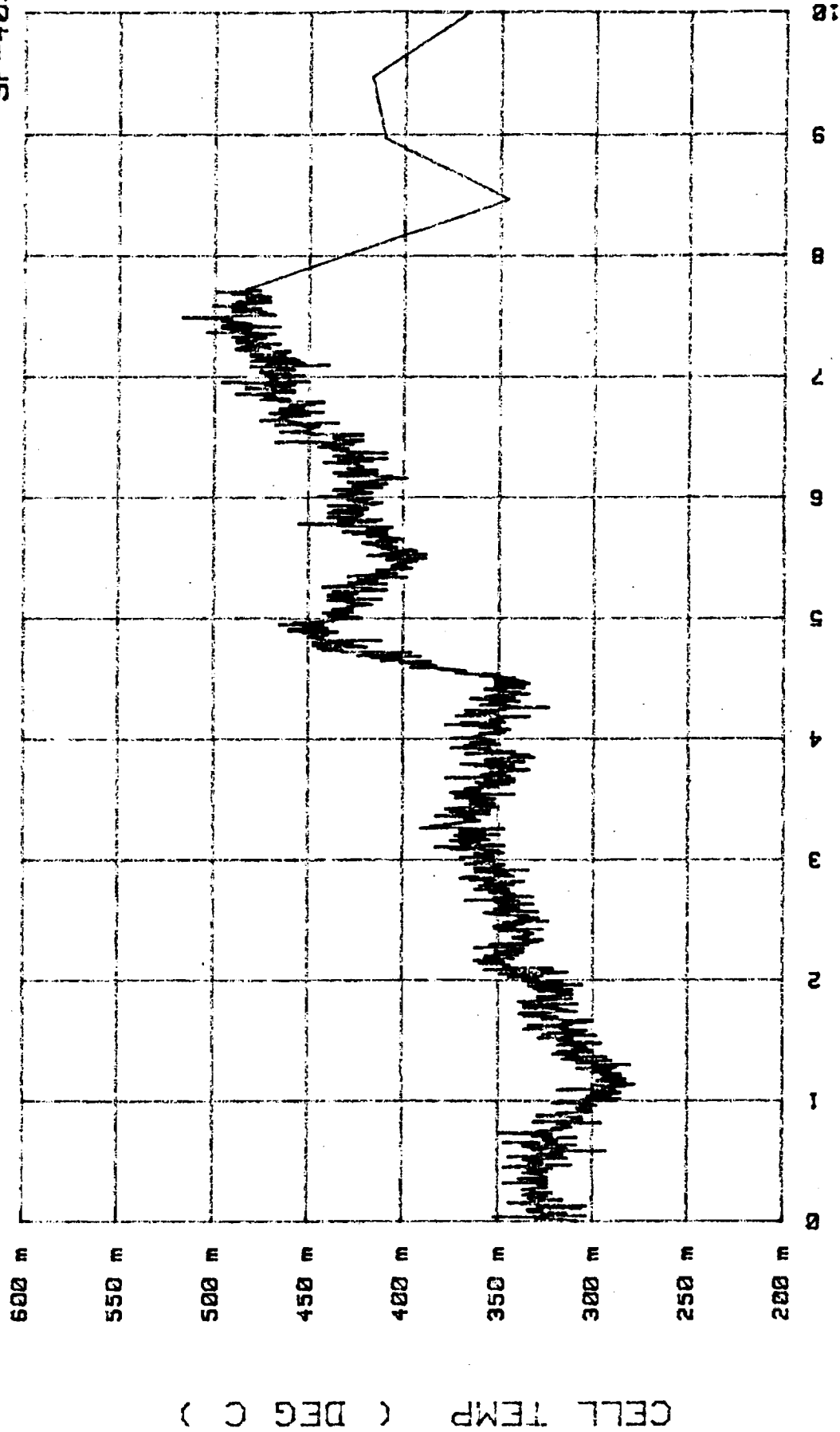


FIG. P4

LI/SOCI2 CELL PERFORMANCE TEST

CELL #1

12 Dec 1995
SF-409



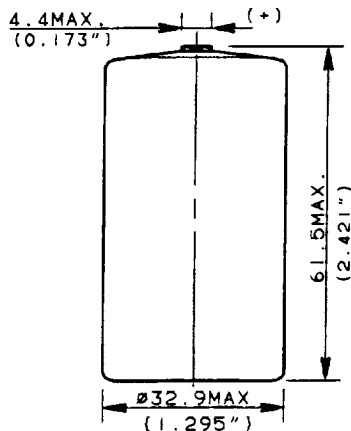
TADIRAN® LITHIUM INORGANIC BATTERIES

LITHIUM XTRA™

MODEL TL-2300

INTERNATIONAL SIZE REFS: D, R20, UM-1

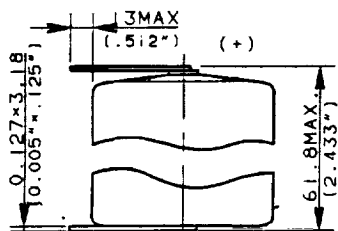
ORDERING INFORMATION:



PRESSURE CONTACT TERMINALS

MODEL: TL-2300/S

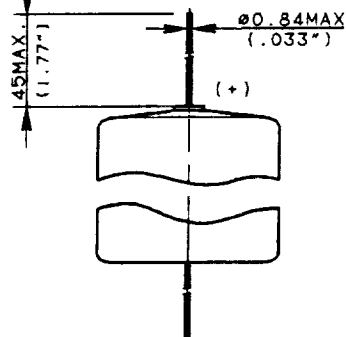
CATALOG NO: 15513021500



FLAT NICKEL STRIP TERMINALS

MODEL: TL-2300/T

CATALOG NO: 15513031500



TIN-PLATED COPPER WIRE TERMINALS

MODEL: TL-2300/P

CATALOG NO: 15513041500

NOTE:

- DIMENSIONS ARE IN MM. AND (IN)
- SPECIAL TERMINALS OR MULTICELL BATTERIES ARE AVAILABLE ON REQUEST.

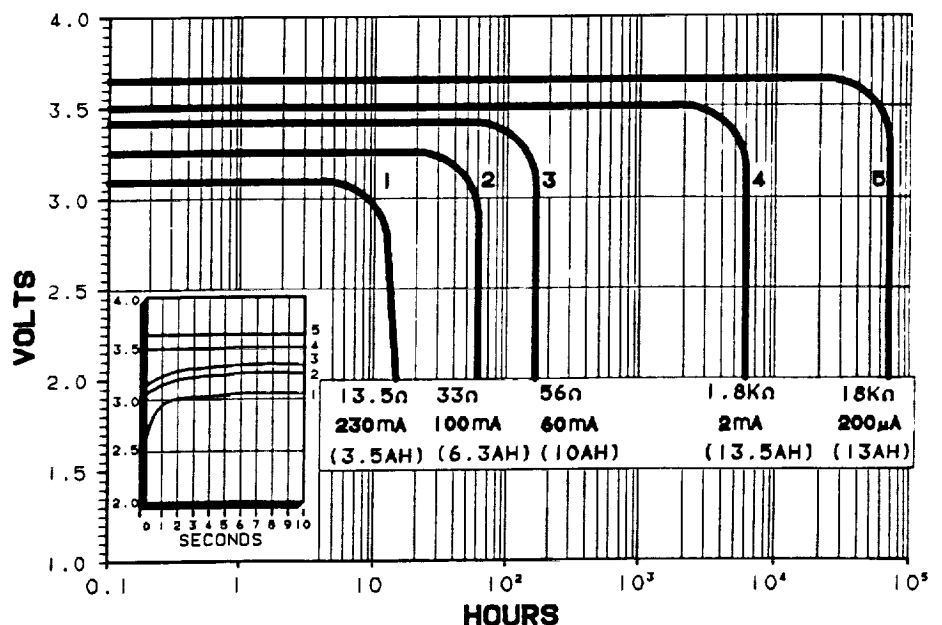


U.L. COMPONENT RECOGNITION
MH 12193

PERFORMANCE DATA: (AT 25°C)

- NOMINAL CAPACITY (AT 2mA TO 2V) 13.5 AH
- RATED VOLTAGE 3.6 V
- MAXIMUM CONTINUOUS CURRENT 230 mA
- PULSE CURRENT CAPABILITY 500 mA
- WEIGHT 100 GR. (3.52 OZ.)
- VOLUME 51 cm³ (3.11 in³)
- OPERATING TEMPERATURE -55°C TO +55°C

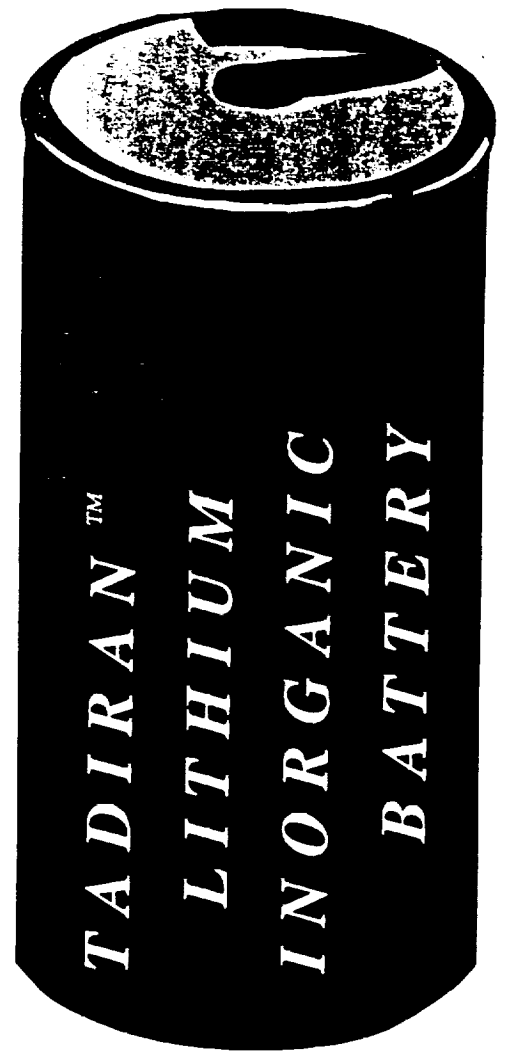
DISCHARGE CHARACTERISTICS AT 25°C



NOTES:

- THE INFORMATION PROVIDED HERE IS NECESSARILY OF A GENERAL NATURE. SINCE SPECIFIC PERFORMANCE DEPENDS ON ACTUAL OPERATING AND STORAGE CONDITIONS, OUR ENGINEERS WILL PROVIDE PARTICULAR APPLICATION INSTRUCTIONS UPON REQUEST.
- DATA SUBJECT TO REVISION WITHOUT NOTICE.
- ANY REPRESENTATIONS IN THIS BROCHURE CONCERNING PERFORMANCE ARE FOR INFORMATIONAL PURPOSES ONLY AND NOT WARRANTIES, EITHER EXPRESS OR IMPLIED, OF FUTURE PERFORMANCE. TADIRAN'S STANDARD LIMITED WARRANTY, STATED IN ITS SALES CONTRACT OR ORDER CONFIRMATION FORM IS THE ONLY WARRANTY OFFERED BY TADIRAN.

MEDIUM POWER



LITHIUM THIONYL CHLORIDE BATTERIES

TADIRAN 

CONTENTS

	Page
1 BASIC INFORMATION	1
1.1 Introduction	1
1.2 Advantages	1
1.3 Cell Chemistry	2
1.4 Applications	2
1.5 Multicell Batteries	2
1.6 Cell Disposal	3
2 ELECTROCHEMICAL SYSTEM	4
2.1 General Description	4
2.2 Cell Components (Fig. 2.1)	4
3 PERFORMANCE	6
3.1 Introduction	6
3.2 Discharge Curves	6
3.3 Cell Capacities	6
3.4 Operating Voltages	6
3.5 Voltage Response	6
3.6 Current Response	8
3.7 Shelf Life	8
3.8 Battery Orientation	9
4 RELIABILITY AND SAFETY	10
4.1 General	10
4.2 Environmental Testing	10
4.3 Safety	10
4.4 Handling Procedures	11

LIST OF ILLUSTRATIONS

Fig.	Title	Page
1.1	Discharge profiles of primary and secondary batteries	1
1.2	Shelf life characteristics of various battery systems	2
1.3	Effect of temperature on gravimetric density of primary and secondary cells ("D" size)	2
2.1	Cross section of medium power lithium cell ("D" size)	4
2.2	Polyswitch resistance-temperature characteristic	5
3.1	Discharge curve for 100 mA discharge current	6
3.2	Discharge curve for 250 mA discharge current	6
3.3	Discharge curve for 500 mA discharge current	6
3.4	Transient voltage curves	7
3.5	Cell capacity versus temperature	7
3.6	Cell capacity versus discharge current	7
3.7	Cell voltage versus temperature	7
	erating voltage at 1 Amp pulse (3% max duty cycle)	8
	Cell capacity versus storage time at 25°C	9
4.1	Short-circuit current-time characteristics	10

CHAPTER 1

BASIC INFORMATION

1.1 Introduction

Tadiran[®] Lithium Thionyl Chloride (LTC) batteries had their market baptism in the early 1970's. In the interim, these batteries have become established among low power standard sources for microelectronic circuits, notably CMOS memories and real time clocks.

These batteries provide a safe and reliable, lightweight power source able to perform for long periods over a wide range of environmental conditions.

And now, Tadiran is offering a new family of Medium Rate/Medium Power (MP) LTC batteries to extend the performance of its present LTC battery line. MP LTC batteries supply higher currents and can thus serve as main power sources to a host of devices over a wide range of applications. MP LTC "D" size cells are being regularly manufactured for single cell or custom battery markets.

1.2 Advantages

Major advantages of Tadiran MP LTC batteries are:

High Cell Voltage. The cell open-circuit voltage of 3.7 V and typical operating voltage of 3.4 V are considerably higher than for other commercially available primary batteries.

Wide Operating Temperature Range. The battery can operate at temperatures from -55 to +65°C.

High Energy Density. The battery has the highest energy density of any available primary battery: up to 420 Wh/kg and 800 Wh/liter.

Long Shelf Life. The especially low self-discharge characteristics and hermetic construction are the basis for the battery's projected shelf life of over 5 years at room temperatures.

Safety. MP LTC cell's hermetic seal ensure total insulation of the chemical constituents where interaction with the atmosphere (usually air) is prohibited. The non-pressurized electrochemical system enhances cell safety.

Polyswitch protection prevents accidental short-circuiting. The cells can withstand arbitrary charge or forced discharge over the entire

temperature range and for working currents. An additional safety measure is provided by an inside vent.

Fig 1.1 compares typical discharge curves for different battery types. The superior performance of the Li/SOCl₂ (LTC) system is self-evident.

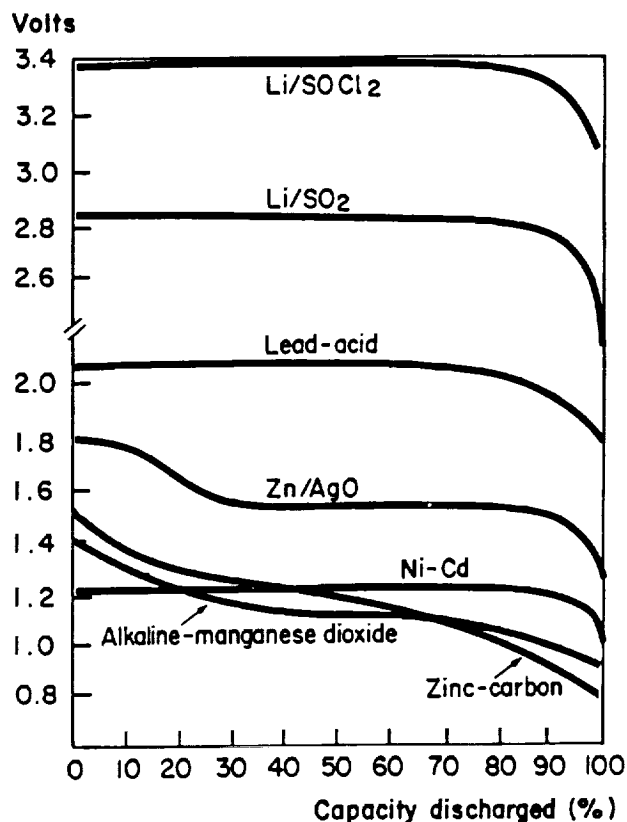


Fig 1.1 Discharge profiles of primary and secondary batteries.

Fig 1.2 illustrates the longer shelf life of Li/SOCl₂ batteries over other electrochemical systems.

The relatively higher energy density of Li/SOCl₂ batteries shown in Fig 1.3, allows for compact battery construction.

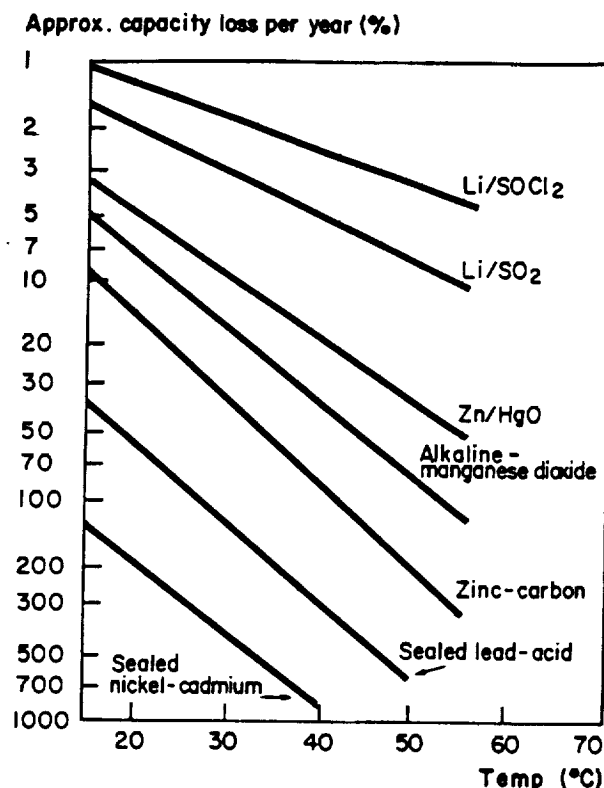


Fig 1.2 Shelf life characteristics of various battery systems

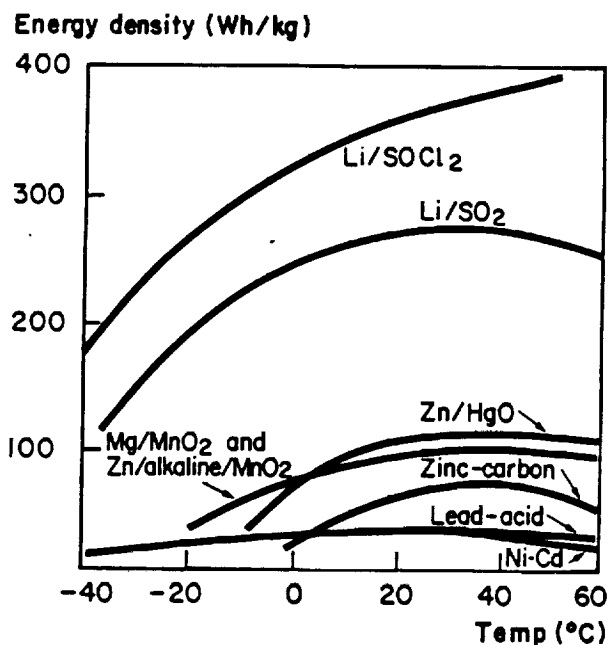


Fig 1.3 Effect of temperature on gravimetric density of primary and secondary cells ("D" size)

1.3 Cell Chemistry

The basic cell chemistry of Tadiran MP LTC cells is similar to that of Tadiran's bobbin LTC cells. Each cell consists of a Lithium (Li) anode, carbon (C) cathode and a solution of aluminum Chloride in thionyl chloride. In common with all Tadiran LTC batteries, the long shelf life of MP cells arises from the formation of a thin layer of LiCl on the anode during the initial reaction between Li and SOCl₂. This layer prevents further reaction or loss of capacity during storage. Anode corrosion, sometimes occurring in aqueous systems, is thus avoided.

The protective layer on the anode may cause voltage buildup delay under relatively high loads or extended storage at high temperatures. This delay however is absent in "milliampere" applications, becoming more pronounced with higher loads (hundreds of milliamperes) or lower operating temperatures. Storage conditions also play a part, particularly high temperatures and extensive duration causing greater delay.

1.4 Applications

The Tadiran MP LTC battery electrochemical system combines the highest packaged density of a commercially available system with a working voltage of approximately 3.4 V, outstanding storage capability and low self-discharge rates (even at temperatures up to 65°C). The unique features of the MP LTC battery and its intrinsic economic benefits give Tadiran's MP LTC batteries the edge in a wide range of applications especially those demanding high reliability when operating under severe environmental conditions.

1.5 Multicell Batteries

Battery assembly based upon series and parallel cell connection¹ is subject to the following recommendations:

- The cells should be interconnected in series by soldering or welding of the flat strips or pins connected to the cell terminals. This avoids overheating that could occur from direct attachment to the cell case.

¹ Having passed Acceptance Testing

- b. When cells are connected in series/parallel combination, a diode should be connected in series with each set of series-connected cells.
- c. A slow-blow fuse should be connected in series with the load wherever several series of batteries are connected in parallel.

1.6 Cell Disposal

Unlike Mercury or Nickel Cadmium batteries, Tadiran's MP LTC cell contains no material with any lasting toxic environmental effect.

However, the cell does contain corrosive materials that will ultimately decompose to form harmless substances. To avoid injury or damage during decomposition, safety procedures should be adopted to neutralize the corrosive materials. These procedures should be initiated for mechanically damaged cells and cells that have not completely discharged. Details of these procedures are included in Tadiran's instructions for handling MP LTC batteries.

CHAPTER 2

ELECTROCHEMICAL SYSTEM

2.1 General Description

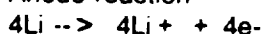
Primary lithium inorganic batteries have been produced by Tadiran since the early 1970's. These batteries have been well publicized by Tadiran and written about extensively in both scientific and patent literature.

The bulk of Tadiran's worldwide lithium battery sales has been of bobbin structure type cells, providing users with safe, explosion hazard-free energy sources. Meanwhile, Tadiran has continued with its R&D efforts toward LTC batteries featuring higher power output, particularly spiral-wound cells. Despite the highly satisfactory electrical performance of these cells, the product was not entirely risk-free and therefore has been withheld from market exposure.

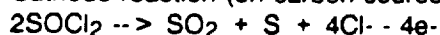
A recently completed intermediate design has been adopted for Tadiran's new medium rate (or medium power) cells now on offer. These cells have a very high safety level and are explosion hazard-free. New MP LTC cells incorporate the basic electromechanical system of Tadiran's conventional bobbin-type LTC cells.

Most quoted half cell reactions during current flow are:

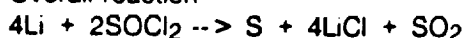
Anode reaction



Cathode reaction (on carbon source)



Overall reaction



Most of the sulfur dioxide formed during cell discharge is dissolved in the electrolyte (attributed to partial chemical bonds). Hence the exceptional properties of LTC cells notably, low internal pressure within the cell both before, during and following cell discharge.

The MP LTC cell discharge mechanism does not cause gas pressure at nominal operating currents.

2.2 Cell Components (Fig. 2.1)

Anode

The anode is made up of battery grade lithium foil, pressed on to a nickel strip current collector that in turn is welded to the battery can. This ensures reliable electrical and mechanical contact.

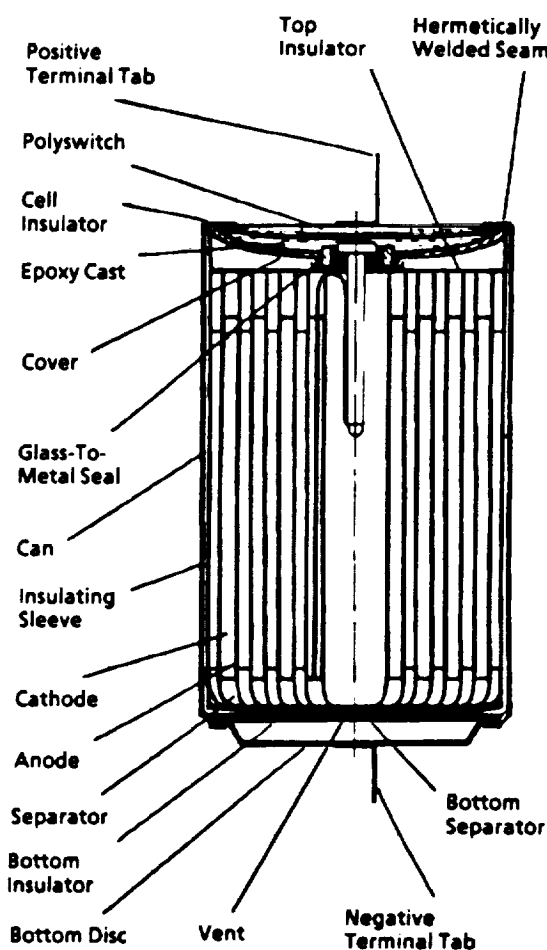


Fig 2.1 Cross section of medium power lithium cell ("D" size)

Separator

The separator located between the anode and the cathode prevents internal short circuiting while enabling ions to move freely between electrodes. The separator is made out of non-woven glass, carefully selected for compatibility with the chemical system during extensive storage and operation.

Cathode

The cathode is made of highly porous teflon-bonded carbon sandwiched onto a nickel screen current collector. Thionyl chloride cathodic reduction occurs on this surface when connected across a load.

The carbon, a catalyst in the chemical reaction, may determine cell capacity when insoluble LiCl (a reduction product) precipitate blocks the carbon pore structure. This flexible structure maintains a minimum separation between anode and cathode during discharge, enhancing mechanical stability (e.g. resistance to shock, acceleration and vibration).

Electrolyte

The electrolyte is primarily a solution of lithium aluminum tetrachloride in thionyl chloride. The electrolyte's electrical conductivity decreases marginally with temperature. The slight temperature gradient, single voltage discharge level of the cell and absence of mass transport control problems, all contribute to the outstanding voltage stability of the Li/SOCl₂ system. The low freezing point of the electrolyte (below -110°C) and relatively high boiling point (above +80°C) have opened the way to production of a medium power battery capable of efficient operation over a wide temperature range (e.g. -55 to +65°C).

Hermetic Package

Hermetic packaging ensures battery shelf life and protection of the equipment in which the battery is installed. Minimum hermeticity level obtained is approximately 10⁻⁸ cm³ He-atm/s.

This is achieved as follows:

Can and Cover. Made of nickel-plated cold-rolled steel, cathodically protected by the lithium metal. The can is designed to withstand the mechanical stresses encountered over the expected wide range of environmental conditions of service.

Welded Seam. The cover is welded to the can by either a TIG, plasma or laser welding process. The mechanical strength of the welded seam is equivalent to the strength of the total package.

Glass-to-Metal Seal. A glass bead is used to insulate the positive terminal from the negative cover. Compression sealing technology ensures good hermeticity and mechanical integrity.

Polyswitch

The MP LTC cell comprises a polyswitch, a Positive Temperature Coefficient (PTC) resistor, designed to protect the cell against short circuiting or high current drain by switching to open circuit and thus avoiding battery overheating. Having cooled down, the battery is automatically reconnected to the load.

Fig. 2.2 shows the polyswitch resistance-temperature characteristic. The graph emphasizes the marked increase in resistance above a given temperature range of several orders of magnitude, taking up most of the circuit voltage drop.

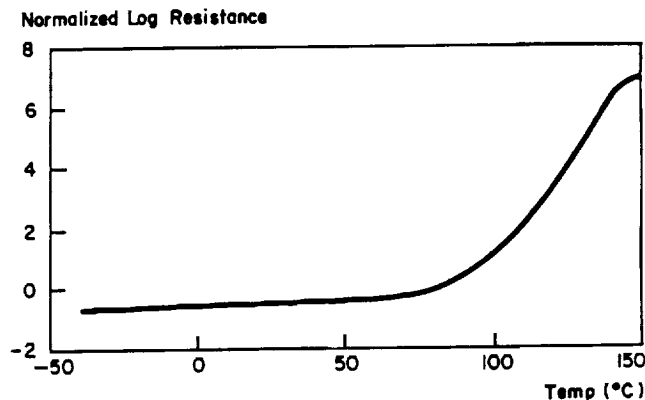


Fig 2.2 Polyswitch resistance-temperature characteristic

Vent

An additional safety measure is provided by a vent incorporated into the lower cell structure. The vent is activated only when the polyswitch fails to respond or cell temperature tops 90°C.

CHAPTER 3 PERFORMANCE

3.1 Introduction

The discharge performance of Tadiran MP LTC cells is dependent upon load current, operating temperature, storage time and conditions prevailing before the onset of discharge.

General cell behavior information is given in the following sections. While specific discharge data for "D" size cells are presented, other cells will perform similarly.

3.2 Discharge Curves

Figures 3.1, 3.2 and 3.3 show typical discharge curves as a function of load current for various ambient temperatures: RT (25°C), High (+65°C) and Low (-40°C).

3.3 Cell Capacities

Fig 3.5 shows the capacity (to 2.0 V) of a "D" size MP LTC cell as function of discharge (ambient) temperature, for specific discharge currents.

Fig 3.6 presents cell capacity as a function of discharge current at constant temperature.

3.4 Operating Voltages

Fig 3.7 shows typical MP LTC cell ("D" size cell) operating voltage as a function of discharge temperature for various discharge currents.

3.5 Voltage Response

On application of a load, the LTC cell voltage drops from open circuit voltage to an operating plateau voltage which is a function of the output current. In most cases the voltage level will stabilize instantly. However, at relatively high currents and particularly at low temperatures, there may be a transition period, in which the initial voltage will drop below the plateau voltage before recovering.

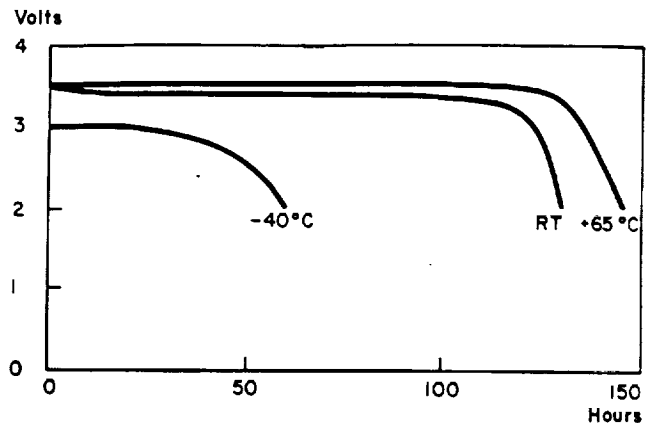


Fig 3.1 Discharge curve for 100 mA discharge current

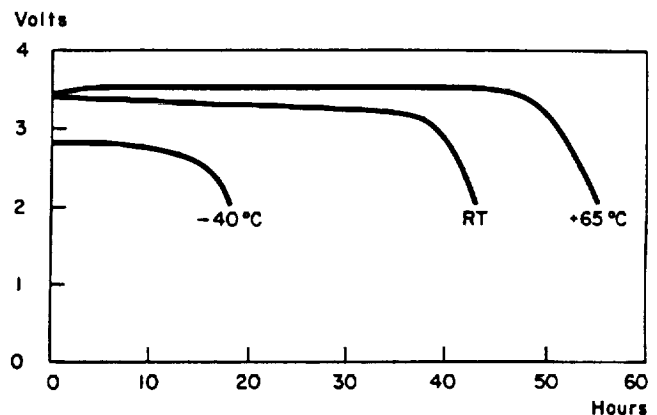


Fig 3.2 Discharge curve for 250 mA discharge current

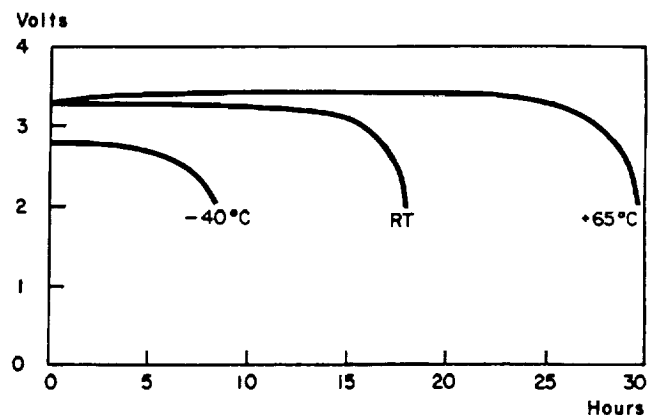


Fig 3.3 Discharge curve for 500 mA discharge current

Figure 3.4 shows three curves indicating initial discharge conditions:

- Instant voltage stabilization at the plateau level.
- A transition period, in which the initial voltage falls below the plateau level, while the minimum voltage is higher than the cutoff voltage. This corresponds to medium currents.
- A delay time, in which the initial voltage falls below the cutoff voltage. This corresponds to high currents.

In Curve 'C', the time to cutoff voltage is referred to as the delay time, which is a feature of lithium battery systems. The lowest voltage reached is referred to as the Transient Minimum Voltage (TMV).

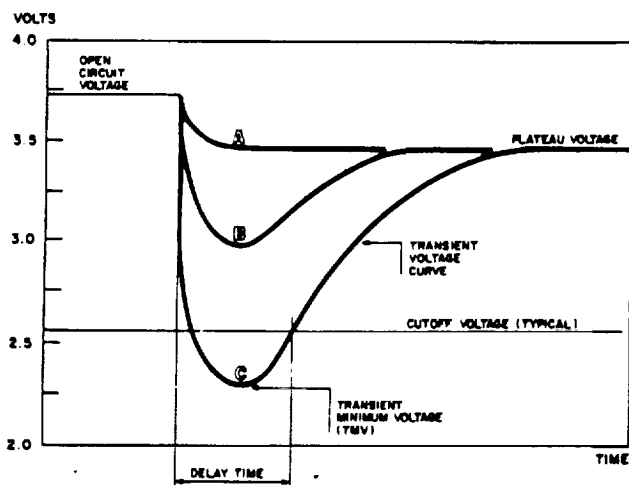


Fig 3.4 Transient voltage curves

Voltage delay in MP LTC cells is caused by the formation of a passivation film of LiCl on the lithium surface. The thickness of the film increases as the storage time and temperature are increased. This film, while preventing a chemical reaction between thionyl chloride and lithium metal, limits the transport of lithium ions from the metal surface to the electrolyte. This causes a temporary increase in the internal ohmic resistance of the cell. Beyond certain current densities, the increased internal resistance will reduce the operating voltage. Once cell discharge starts, the passivation film is dissipated gradually, the internal resistance returns to its nominal value and plateau voltage attained.

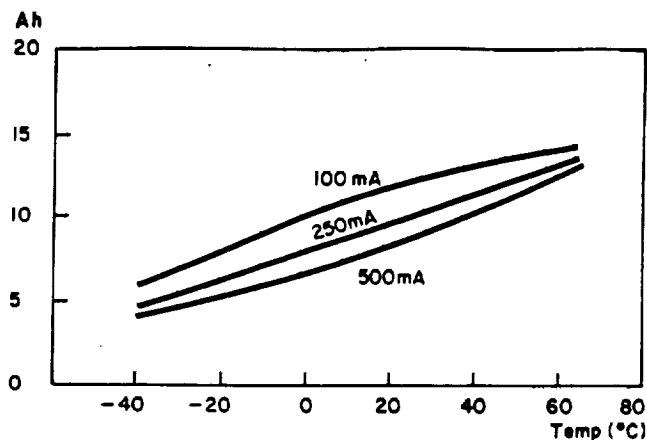


Fig 3.5 Cell capacity versus temperature

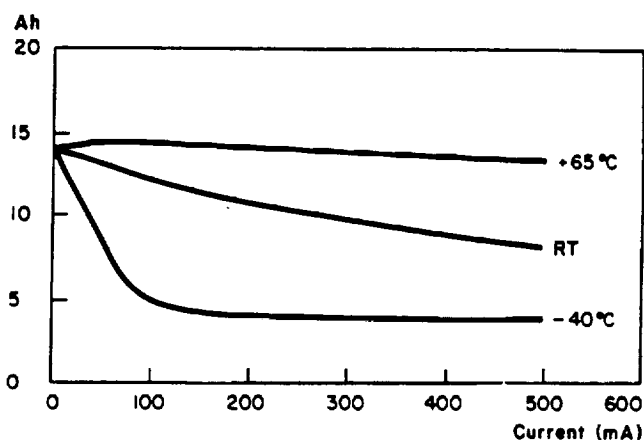


Fig 3.6 Cell capacity versus discharge current

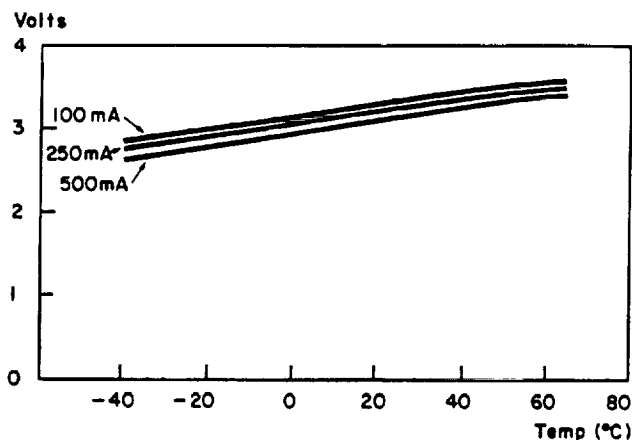


Fig 3.7 Cell voltage versus temperature

For low and medium discharge currents, the ionic conductivity of the LiCl film is sufficient to maintain a relatively free flux of lithium ions. If the current is higher, the film begins to limit the ion flow. Reducing the temperature produces a decrease in ionic conductivity with similar results.

Once the passivation film is dissipated, it will rebuild itself only if the cell is again subjected to identical storage time and temperature conditions to those which resulted in the previous passivation.

The following performance data for "D" size MP LTC cells, after one year's storage at room temperature, illustrates voltage response of MP LTC cells in the three discharge ranges described above:

- For discharge currents up to 30 mA, the nominal cell voltage will exceed 3.4 V at all times.
- For discharge currents up to 60 mA, nominal cell voltage may drop below 3.4 V, but always remain above 3.0 V. For higher currents, up to 100 mA, recovery time to 3.0 V and above will be less than 10 seconds.
- For discharge currents up to 250 mA, nominal cell voltage will reach 2.8 V in less than 10 seconds from time of load-cell connection and remain above 2.8 V at all times.
- For higher discharge currents up to 500 mA, cell voltage will recover to 2.5 V and above in less than 10 seconds.

3.6 Current response

Continuous Current

The maximum allowable continuous operating current for "D" size cells, is 500 mA. Prolonged operation at higher currents may heat up the cells, causing the polyswitch to become activated.

The following table lists the "hold" and "trip" currents for MP LTC cells at different temperatures. The "hold" current flows through the cell without tripping the switch. A current flow in excess of a critical tripping current value will shift the polyswitch from "hold" to "tripped" state.

This will markedly reduce the current flowing through the cell and prevent a rise in cell temperature.

Temp (°C)	I-hold (Amperes)	I-trip (Amperes)
65	0.7	1.3
20	1.0	2.2
- 40	2.0	5.0

Pulses

In addition to providing continuous current, MP LTC cells are capable of pulsing higher currents when required.

Fig 3.8 shows the operating voltage of a "D" size cell at room temperature as a function of pulse width for a 1 ampere pulse.

Cell voltage exceeds 3.0 V over the entire range.

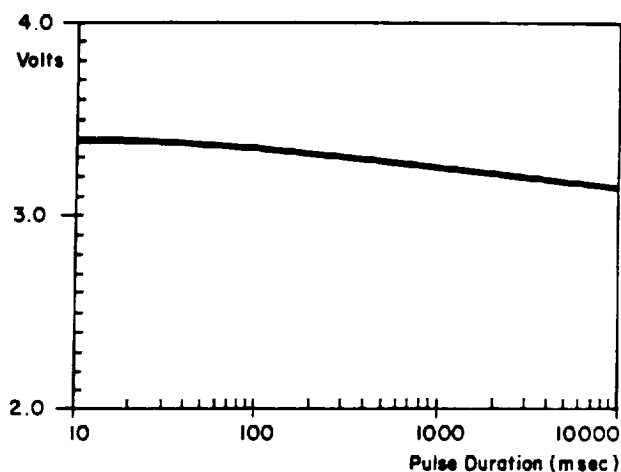


Fig 3.8 Operating voltage at 1 Amp pulse (3% max duty cycle)

3.7 Shelf Life

The long shelf life of Tadiran MP LTC cells is a result of the high stability of the lithium anode in contact with the thionyl chloride (LiCl passivation film) and from the high activation energy of the lithium in the inorganic system.

Another factor contributing to the long shelf life is the high stability of the other cell components in thionyl chloride. For example, the can and cover are given cathodic protection by the lithium, before, during and after cell discharge. The carbon, the nickel screen current collector and the separator glass fiber are all inert in the electrolyte.

Accelerated life tests performed on Tadiran MP LTC cells show that long shelf life with high capacity retention can be expected. Storage capacity loss of just 2 to 3% per annum is forecast at room temperature. MP LTC cells stored for 3 months at 65°C, experienced capacity loss of less than 10%.

The basic electrochemical system of Tadiran MP LTC cells is the same as that of Tadiran LTC bobbin type cells. Therefore, a similar shelf life behavioral pattern may be expected. Storage tests made at various intervals during 10 years manufacturing LTC cells, confirm insignificant capacity losses.

Fig 3.9 shows a typical capacity curve obtained for cylindrical bobbin type LTC cells under shelf life testing at 25°C, over a ten year period at rated discharge currents. The curve is indicative of all Tadiran LTC cells.

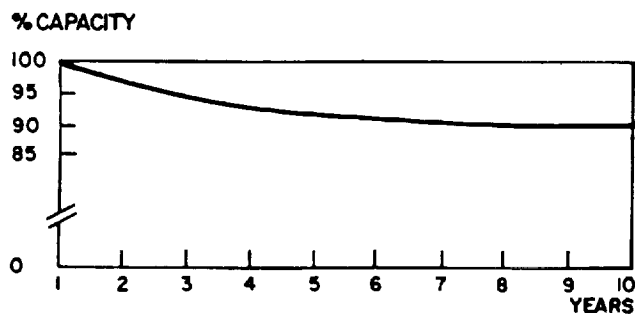


Fig 3.9 Cell capacity versus storage time at 25°C

3.8 Battery Orientation

Often, a battery's electrical performance, particularly with respect to cell capacity, is dependent upon its orientation during discharge: upright, horizontal or inverted positions.

Not so in the case of Tadiran MP LTC batteries. Capacity of "D" size cells, for example, was identical in both "up" and "down" positions for 100 mA and 250 mA discharge currents (at 25°C).

In the horizontal position, the capacity was found to be within 5% of the "up" and "down" values.

CHAPTER 4

RELIABILITY AND SAFETY

4.1 General

Tadiran MP LTC cells have brought about the development of compact, light weight, medium rate/medium power high energy source batteries, with characteristic long shelf life, wide operating temperature range and flat discharge curve.

Electrochemical power sources exhibiting top-of-the-line features contain powerful reducing and oxidizing materials. It is therefore incumbent upon battery manufacturers to provide a product that is both reliable and safe under normal operating conditions.

Tadiran MP LTC batteries have undergone rigorous test programs to ensure long-term reliability and safety. These programs follow American military standards and specifications as detailed below. Tadiran MP LTC batteries complied with the most stringent requirements.

4.2 Environmental Testing

MP LTC cells are required to meet both physical and electrical specifications while being subjected to the following environmental tests:

- Vibration as per MIL B-49461 ER Para 3.9
- Mechanical Shock as per MIL B-49461 ER Para 3.10
- Drop as per MIL B-49461 ER Para 3.11
- Altitude as per MIL B-49461 ER Para 3.12
- Bounce as per MIL 810 C Method 514.2 Procedure XI Part 2
- Humidity as per MIL STD 202 E Method 103 B
- Temperature Cycle as per MIL STD 810 C Method 501.1 Procedure II and Method 502.1 Procedure I

4.3 Safety

Tadiran MP LTC cells are designed to be explosion hazard-free. This, by optimizing the cell's constituents and incorporation of two additional safety features, a polyswitch and safety vent:

Polyswitch

The polyswitch is activated in the event of external shorting or high drain rate occurrence beyond the maximum MP cell rating. Fig 4.1 shows typical short circuit (SC) current-time characteristics for an MP LTC cell for different temperatures. The decrease in short circuit

current is such that cell temperature does not exceed 75°C, even when the ambient temperature is as high as 65°C.

Safety Vent

The safety vent is activated when the cell is subject to:

- a. Compression.
- b. Temperatures above 100°C.
- c. Incineration of a fully-charged cell.

The vent will not be activated with short-circuiting (the polyswitch will respond in this event, disconnecting the circuit).

"D" size cells were tested as follows:

- Each cell was reversed at currents up to 500 mA for 24 hours at -40°C, RT and +65°C, without safety vent activation.
- Each cell was charged at currents up to 500 mA for 24 hours at -40°C, RT and +65°C, without safety vent activation.

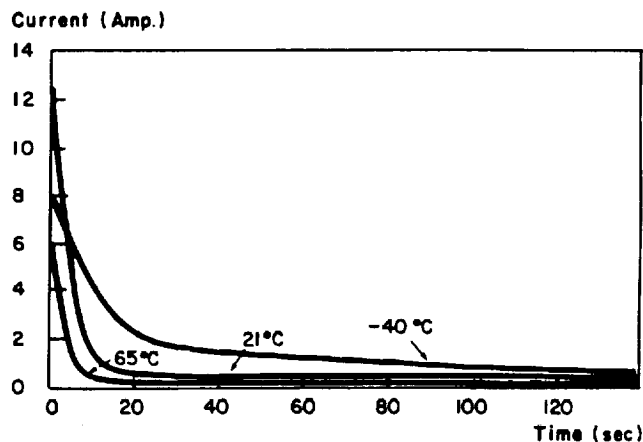


Fig 4.1 Short-circuit current-time characteristics

Handling Procedures

Lithium batteries are a relatively recent power source and consequently, customers often require qualified advice and instruction on their correct usage.

The following handling instructions pay close attention to the different attributes required by end-users and/or OEM's when applying MP LTC batteries, particularly the supply of specified current and energy to equipment under all reasonable operating conditions. In addition, batteries should be:

- Reliable and maintenance-free.
- Safe.
- Cost-effective.
- Compact.

The handling instructions are broken down into the following sections:

- Acceptance testing.
- Storage.
- Fire extinguishing.
- Cell assembly.
- Transportation.
- Disposal.

Acceptance test procedure

Acceptance testing of cells begins with visual inspection of incoming items. Cells that are mechanically damaged, rusty or show signs of leakage residue should be discarded.

The Open Circuit Voltage (OCV) of the remaining cells should then be measured by digital voltmeter having a minimum input impedance of 10 Meg-ohm and minimum resolution of $3\frac{1}{2}$ digits, retaining only cells, whose open circuit voltage is equal to or greater than 3.66 V. OCV cell variations are sometimes related to the manufacturing process. Also, cell OCV depends upon storage time and environmental conditions (e.g. temperature) with the result that testing of a random sample of cells will produce a distribution of OCV values. An internally defective cell will usually result in cell self-discharge, which in turn will reduce the measured OCV below the minimum acceptable level of 3.66 V. These cells should be rejected.

As the discharge curve of Tadiran LTC cells is predominantly flat, neither open circuit voltage nor loaded cell voltage may be employed to determine cell residual capacity.

Storage

- *General*

Lithium batteries should be stored in their original packaging materials. This will eliminate unintentional cell shorting and/or shorting between cells.

With large storage volume (thousand's of batteries), a well ventilated, low humidity environment is recommended.

- *Fire extinguishers*

Metal X and Lith X fire extinguishers are recommended. The stand should incorporate CO₂ and Lith X fire extinguishers, a minimum of two gas masks with SO₂ filters, a protective helmet and gloves to withstand heat.

Fire extinguishing

Lithium X fire extinguishers should be used to fight fires involving lithium batteries. Otherwise, CO₂ extinguishers may be used.

**Water should never be used on fires
in the presence of lithium batteries**

Assembly of Cells

Battery assembly based upon series and parallel cell connection¹ is subject to the following recommendations:

- a. The open circuit voltage of cells should be measured prior to battery assembly by digital voltmeter having a minimum input impedance of 10 Meg-ohm. Only cells whose OCV is equal to or greater than 3.66 V are suitable for battery assembly.
- b. The cells should be interconnected in series by soldering or welding of the flat strips or pins connected to the cell terminals. This avoids overheating that could occur from direct attachment to the cell case.
- c. When cells are connected in parallel a diode should be connected in series with each set of series-connected cells connected together in parallel.
- d. A slow-blow fuse should be connected in series with the load wherever several series of batteries are connected in parallel.

Transportation

Tadiran's recommendations for the safe and legally acceptable transportation of Lithium batteries are based upon regulations issued by the following national and international bodies:

US Department of Transportation

The Federal Department of Transportation's title 49 code of regulations (49 CFR), parts 100-199, governing all domestic shipment of hazardous materials (specifically para. 173.206)

IATA

The International Air Transport Association's IATA restricted article regulations for shared control with ICAO (see below) of international air shipment of hazardous materials.

ICAO

The International Civil Aviation Organization's technical instructions for the safe air transportation of dangerous goods.

According to IATA, Tadiran MP LTC cells, containing more than 0.5 g of lithium metal, are restricted articles requiring appropriate documentation, packaging and labelling.

¹ Having passed Acceptance Testing.

While passenger aircraft shipment is forbidden, cargo aircraft shipment is permissible, subject to compliance with DOT-E-7052. The latter ensures meeting both IATA and ICAO requirements.

Tadiran has been granted US DOT-E-7052 exemption (see below) enabling both cargo aircraft and overland shipment of MP LTC cells and batteries.

Under US DOT-E-7052 exemption, LTC cells of Tadiran manufacture may be shipped within the US and internationally (wherever the validity of exemption is recognized). The exemption specifies packaging, labelling and documentation requirements. Both shipper and receiver of goods should have copies of DOT-E-7052 at hand, at all times, to ensure strict adherence to the provisions of the exemption.

Devices containing MP LTC batteries require specific identification and written acknowledgment by the US Office of Hazardous Materials Regulations (OHMR) prior to initial shipment.

DOT-E-7052 relates exclusively to the transportation of unused or partially discharged cells having an open circuit voltage in excess of 2.0 V. Transportation of discharged cells and batteries is covered by DOT-CFR 49F waste regulations.

As IATA, ICAO and US DOT regulations for transportation of lithium batteries are periodically revised, updated information should be sought from Tadiran or the appropriate agency from time to time.

Disposal

Unlike mercury or nickel cadmium batteries, Tadiran MP LTC cells are devoid of material having any lasting toxic environmental effect. However, corrosive materials that are present, will ultimately decompose and form harmless substances. To avoid any personal injury or damage during decomposition, safety procedures should be adopted to neutralize the corrosive materials.

The flammable, solid lithium anode and toxicity of the electrolyte fumes, demand that completely discharged, mechanically damaged cells be wrapped in strong packing material prior to disposal.

Small to medium (up to hundreds of kilograms) quantities of MP LTC batteries may be disposed of by burial in landfills. The batteries should be placed in plastic bags containing a neutralizing agent e.g. calcium carbonate (CaCO_3) while the landfill location should conform to local statutory regulations.

Large quantities of lithium batteries should be disposed of by professional waste disposal agencies in accordance with local and national regulations.

SUPPLEMENTARY APPENDICES

- Appendix A: Summer Project Schedule
- Appendix B: Mission Profile
- Appendix C: Micro-Met Mission - Science Objectives and Mission Design Drivers
- Appendix D: Test Plan
- Appendix E: Communications System Design Specifications (Mars Data Relay protocol)
- Appendix F: Pressure Sensor Development Plan
- Appendix G: Micro-Met Prototype Power Subsystem
- Appendix H: Meeting Notes --
 - June 30, 1995
 - July 5, 1995
 - July 12, 1995
 - PDR** (July 21, 1995)
 - August 23, 1995
 - CDR** (August 29, 1995)

SUMMER PROJECT SCHEDULE

Deadline	Task
<hr/>	
30 June	Schedule & Design Discussion
<hr/>	
07 July	Concept refinement
<hr/>	
14 July	Procure TNC's Begin building external timer
<hr/>	
17 July	Begin NMI board testing; Begin power subsystem design Begin communications interface design
<hr/>	
21 July	Preliminary Design Review, at Ames Begin software implementation Implement communications interface
<hr/>	
28 July	Complete power subsystem design, Identify and procure hardware for next design iteration Demonstrate link through TNC's
<hr/>	
11 August	Integrate D. Catling's sensors Begin work on second iteration (more flight-like)
<hr/>	
21 August	Critical Design Review (Stage 1: Stanford) Freeze second iteration design
<hr/>	
28 August	Critical Design Review (Stage 2: Ames presentation) Demonstrate autonomous operation
<hr/>	
01 September	Design/Test Review
<hr/>	
08 September	Test Status Review
<hr/>	
15 September	Documentation Review
<hr/>	
18 September	Documentation Due
<hr/>	
28 September	InterMarsNet Conference
<hr/>	

◀ Back to MET home page.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 28 12:09 1995 PDT

MISSION PROFILE

Launch and Transfer to Mars

- Launch on Med-Lite booster (490 kg to Mars transfer orbit)
- Carrier Spacecraft carries 16 landers to Mars
- Centrifugal release of 8 stations on hyperbolic approach to Mars
- Boost maneuver
- Centrifugal release of remaining 8 stations

Entry, Descent and Landing

- Hypersonic entry (altitude: 125 km; Speed: 7 km/sec; t = 0 sec)
- Maximum deceleration (20.2 earth G, altitude 28.1 km; t = 62 sec)
- Parachute deployment (altitude: 8.9 km; Speed: Mach 1.8; t = 121 sec)
- Surface impact (Speed: 26 - 35 m/s; t = 215 - 354 sec; 800 - 1600 earth G)

Operating Phase

- 1 pressure and 1 temperature measurement every hour; station goes to low power mode in between measurements
- Receiver turned on at the end of measuring period (30 sols) to wait for orbiter beacon
- Upon orbiter beacon detection, receiver turned off, transmitter turned on, data relayed to orbiter

◀ Back to MET home page.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 13 14:27 1995 PDT

SCIENCE OBJECTIVES AND MISSION DESIGN DRIVERS

MET Research Project Memorandum

Subject: Science Objectives and Surface Station Design Drivers
By: Steve Merrihew
Date: 7/3/95

INTRODUCTION:

This memorandum is intended to summarize the Micro-Met science objectives and describe the principal surface station design drivers. Note that this document is intended to define the design drivers for the Micro-Met surface station element only, not the entire Micro-Met mission (composed of the surface station, the entry, descent and landing subsystems and the carrier spacecraft). Once the surface station design drivers have been identified, the requirements for the Summer term (1995) research project to be conducted by NASA/Ames and Stanford University can be defined.

References:

Haberle, Robert M., "Mars Micro-Met Mission Science, A presentation to The Mars Science Working Group", October 28, 1994

Merrihew, Steven C., "A Mars Micro-Meteorology Station Mission, A Presentation to The Mars Science Working Group", October 28, 1994

SCIENCE OBJECTIVES:

The overall objectives for Mars atmospheric science missions are as follows (Ref. Haberle);

- Describe the time and spatial structure of the general circulation of the martian atmosphere.
- Understand the relationship between the general circulation and the forces that drive it.
- Relate that understanding to the martian climate system.

Specific questions related to the general circulation include (Ref. Haberle);

- What are the distributions and properties of the thermal tides?
- What is the time/space structure of the meridional mass flow and the structure of the meridional overturning circulation?
- What are the properties of midlatitude transient eddies and stationary waves?
- How do small-scale waves and turbulence affect the large-scale flow?
- How do the surface fluxes of heat, momentum, moisture and dust vary in space and time?
- How do all the above vary with forcing?

The Micro-Met mission described here utilizes pressure as the sole science measurement. Pressure is both the most important meteorological parameter and the easiest measurement to make from the martian surface. The contributions of a Micro-Met lander mission to the Mars atmospheric science

objectives (when coupled with an orbiter mission) are as follows (Ref. Haberle);

- Landed measurements give the time varying spatial distribution of atmospheric mass.
- Orbital measurements give the time varying thermal structure and forcing function.
- Conducted simultaneously, these measurements give the full 3- dimensional structure of the general circulation using either the thermal wind relationship or 4-dimensional data assimilation.
- Surface pressure measurements will also define the CO₂ cycle.

SCIENCE REQUIREMENTS:

Given the above stated science objectives, the science requirements for the Micro-Met mission can be defined;

- I. Establish a globally distributed network on the surface of Mars to measure the time varying pressure field.
 - A. at least 12 to 15 stations
 - B. at least +60 to -60 degrees of Latitude
 - C. all Longitudes
- II. Long lived surface stations
 - A. at least one Mars year (687 earth days)
- III. Pressure measurement requirements
 - A. accuracy to at least 0.2%
 - B. precision to at least 0.1%
 - C. at least 25 measurements per sol per station

ENGINEERING REQUIREMENTS:

The Micro-Met mission design includes the following mission components;

- Earth to Mars carrier spacecraft
- Atmospheric entry aeroshell
- Descent and landing subsystems (parachute and crushable material)
- Surface station

The design requirements pertinent to the Micro-Met surface station are as follows (see the attached functional block diagram for subsystem definitions);

- I. Environment
 - A. Earth to Mars transfer -
 - 1) Deep space temperature, radiation
 - B. Entry, Descent and Landing -
 - 1) Peak external temperature approx. TBD
 - 2) Peak entry deceleration approx = 20 earth gees
 - 3) Peak landing deceleration approx. = 1500 earth gees
 - C. Surface Operations (see NASA TM 100740 for surface environmental details) -
 - 1) Primarily CO₂ atmosphere at 7 millibars average pressure
 - 2) Surface temperature varies between approx. -110 deg. C and +20 deg. C.
 - 3) Radiation (see NASA TM 100740)

II. Surface Operation

A. Command and Data Handling-

- 1) See Table 1 for data collection requirements.
- 2) Temperature is measured to correct for temperature sensitivity of the pressure sensors. If the selected pressure sensor is not temperature sensitive, then the temperature sensors will be removed (to be studied).
- 3) One measurement of each type (pressure and temperature) is to be recorded from the three sensors provided. This one measurement is to be the most statistically significant parameter. An average is proposed, this is to be studied.
- 4) Logic is to be provided in the data handling subsystem to determine when a sensor has failed. A failed sensor is to be ignored by the data collection subsystem. This logic may include (to be studied);
 - a) indication of a failed sensor to science team
 - b) periodic checks of failed sensor to determine status
 - c) failure determination parameters (% out of tolerance from other sensor, others schemes?)
- 5) Memory should be provided to store up to 6 months of data.

Table 1: Data Collection Plan

Measurement	Word Length (bits)	Digitization Resolution	# Meas. per Sol	Data per Sol (bits/sol)
Pressure (avg. of 3)	12	0.00176 @ 7.0 v	25	300
Temperature (avg. of 3)	8	0.027 @ 7.0 v	25	200
Engineering Data	8	n/a	2	16
Station ID	6	n/a	1	6
Sub Total =				522
20% Margin =				104
TOTAL =				626

B. Communications:

- 1) Communications are to be initiated every 30th Sol as follows -
 - a) receiver commanded on by station timer
 - b) communications orbiter beacon (UHF) received by station
 - c) receiver commanded off (if no beacon received after TBD)
 - d) UHF uplink from station to orbiter, transmission of at
 - d) communications timer reset for another 30 Sols
- 2) Communications protocol -
 - a) Orbiting Mars Relay communication system as baselined

- b) 405 Mhz uplink
 - c) 8 kbits/sec data rate
 - d) two way comm. supported (only beacon required)
- 3) Baseline communications design (to be studied)
- a) 3 Watt input, 1 Watt RF output
 - b) Hemispherical patch antenna (one on each side, "up" side)
 - c) 3dB performance margin ($E_b/N_o = 16$ dB)
- C. Power supply and control:
- 1) Baseline power and energy requirements are shown in Table 2.
 - 2) Lifetime = 1 Mars year (687 days) plus 20% margin
 - 3) Thermal environment approx. = -40 deg C to +40 deg C
(lower temperatures to be studied)
 - 4) Power system activated upon arrival at Mars
 - 5) The baseline battery technology (LiSOCl₂ D-cells) provide

Table 2: Electric Power and Energy Requirements

Sub System	Comm. Day Power (mW)	Comm. Day Energy (mWhrs/Sol)	Non-Comm. Day Power (mW)	Non-Comm. Day Energy (mWhrs/Sol)
Science Instruments	60.0	8.3	60.0	8.3
Communications	3000.0	20.8	0.0	0.0
Command and Data Handling	806.0	207.1	806.0	207.1
Total (including 20% margin) =	4639.2	283.5	1039.2	258.5

III. Integration with Carrier Spacecraft

- 1) Mechanical support provided by carrier s/c
- 2) Electrical support may be provided by carrier s/c (to be studied)
- 3) Thermal control may be provided by carrier s/c (to be studied)

◀ Back to MET home page.

Maintained by: MET team
 Send email to: ssdl@aa.stanford.edu
 Last modified: Jul 12 17:23 1995 PDT

TEST PLAN

Subject: Micro-Met Station Prototype Project Test Plan
By: Steve Merrihew
Date: 7/26/95

INTRODUCTION:

This memorandum is intended to provide a high level test plan for the Micro-Met Surface Station Prototype summer research project. The purposes of the test plan are to answer the following questions;

- 1) How do we know when the project is finished?
- 2) How do we quantitatively evaluate the performance of the prototype?
- 3) What is the best demonstration of the prototype?

These questions will be addressed by this proposed test plan. The student team members are to use this test plan to develop a detailed test program for the summer project.

References:

- 1) Micro-Met Research Project Memorandum, "Science Objectives and Surface Station Design Drivers", by Steve Merrihew, July 7, 1995
- 2) NASA-Ames/Stanford Joint Research Interchange, "A Proposal for a Micro-Met Surface Station Prototype Research Project"

TEST PLAN:

- I. End to end demonstration of functionality (addresses questions 1, 2).
 - A. Science sensor interface (TBD pending David Catling):
 - 1) 0 to +5 V analog input
 - 2) 12 bit pressure A/D
 - 3) 8 bit temperature A/D
 - B. Timer commanded functions:
 - 1) Science data collection events
 - 2) Data manipulation algorithms
 - 3) Sensor diagnostics and engineering telemetry
 - 4) Communications receiver powered on/off
 - C. Orbiter communication beacon commanded functions:
 - 1) Transmit of science data (Lab protocol vs. Mars Relay protocol)
- II. Detailed test report (addresses question 2).
 - A. Interface definitions and demonstration.
 - B. Electric power usage, including warm up requirements.
 - C. Operation of power sub-system in cold temperature case.

NOTE: Specifications of the electronic components used in the prototype (including mass, volume, temperature and radiation tolerance) are to be described in a separate design report.

III. Demonstration (addresses question 3).

- A. Micro-Met surface station prototype transmits autonomously acquired surface data to the Stanford ground station when commanded by a ground station beacon.

B. Optionally establish a real time WWW page link to the transmitted science data.

◀ Back to the MET home page.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 28 14:59 1995 PDT

COMMUNICATIONS SPECIFICATIONS

The Mars Relay Telecommunications document which follows gives a technical description of the parameters to which the Micromet communications system will have to conform. At the prototype stage, we will not fret too much about conforming to this; we are mainly concerned with producing an operational *processor*. Our prototype's comm system can however be inspired by the type of operations detailed below.

Subject: Mars Relay Telecommunications Design Notes
 By: Steve Merrihew
 Date: 7/17/95

INTRODUCTION:

The following is a technical description of the Mars Relay telecommunications system. The Mars Relay (MR) system consists of a master UHF communications system (antenna and transceiver) on board a Mars orbiting spacecraft and subordinate Mars surface station (or balloon or rover etc.) communication systems. The basic document was provided by JPL (all text numbered Section 9.0 and higher), my notes are included in parentheses.

Briefly, the Mars Relay system provides a simple low to medium rate (8,000 and 128,000 bits per second) UHF link (approx. 405 MHz) between a Mars orbiter and any ground station. The orbiter to surface station link sequence is as follows (see Section 9.1.B.2 for details);

- 1) Orbiter transmits a FM beacon at 437.1 MHz with one of three Request Command (RC) subcarriers (to trigger specific landers) when the Orbiter's guidance system determines that a Lander is within view.
- 2) If Lander receives beacon (with appropriate RC subcarrier), the Lander transmits approx. 2 seconds of pure carrier followed by approx. 0.5 seconds of pseudo-random numbers to allow the Orbiter receiver Viterbi decoder to synchronize.
- 3) The Orbiter determines if Lander-Orbiter link is satisfactory (greater than -126 dBm for 8000 bits per second data rate), if so it sends the telemetry command (TC) signal to the Lander.
- 4) After receiving the TC, the Lander transmits its science telemetry to the Orbiter until either loss of signal (at the Orbiter) or the end of the 16 second Balloon Telemetry Time Slot (BTTS). The time available for telemetry transmission is approx. 13 seconds (if the Orbiter is in range). The Lander telemetry is phase modulated with Viterbi coding as an option.

The BTTS is a 16 second communication block (each BTTS repeats steps 1-4). The BTTS is employed as the Lander and Orbiter do not know when the communication event will terminate, so the BTTS "packetizes" the telemetry. The Lander must therefore know which telemetry "packets" have been successfully transmitted after each BTTS.

The Mars Relay is baselined for the Mars Surveyor program. The near term missions are the Mars Global Surveyor and Mars Pathfinder lander (to be launched in 1996) and the Mars Surveyor Orbiter and lander (to be launched in 1998).

9.0 Communications

9.1 Relay (Orbiter) Link

A. UHF relay link communications capability between Mars landers and Earth is provided GFP by the MSP orbiter segment via the Mars Relay (MR) as described in Table 9-1. The lander shall be capable of communicating with both the 1996 MGS and the 1998 Candidate Orbiter.

Table 9-1 MSP Mars-to-Orbiter Relay Link Characteristics

	1996 MGS	1998 Candidate Orbiter
Relay Link Capability	1-way Lander to Orbiter	2-way
Orbit Characteristics	MO Orbit	MO Orbit
Period	1.96h	1.96h
Inclination	92.87°	92.87°
Altitude	351 x 406 km	351 x 406 km
Eccentricity	0.00725	0.00725
Sun Synchronous	Yes	Yes
Repeating Ground Track	No (very long repeat cycle)	No

B. Lander relay links shall be designed to use the following relay link capabilities.

1. The MR uses a 16 s cycle termed BTTS (Balloon Telemetry Time Slot). The BTTS can either : 1) have 14s of Request Command (RC) subcarrier and 2s of pure carrier, if there is no response from a lander, or, 2) if there is a response from a lander, have a transmission cycle of 15s (combination of RC and telemetry command (TC)), followed by 1s of pure carrier. (See Figure 9-1 for link protocol; see Table 9-2 for subcarrier frequencies.)

2. Acquisition/Transmission Sequence

- a. The orbiter via the MR broadcasts a frequency modulated beacon at 437.1000 MHz. The orbiter-to-lander beacon signal is modulated with one of three possible sets of request command (RC). (Table 9.2)

- b. Upon detection of the RC (by the lander), the lander transmits a pure carrier to allow the MR to synchronize to the carrier. This is followed by the lander sending an acquisition preamble (Viterbi PN sequence) that allows the MR to synchronize and lock its Viterbi decoder. This preamble can be any random bit sequence including a sufficient number of convolutionally encoded bits.

- c. After locking the carrier and bit synchronizer, the MR opens a time window and checks for the Viterbi output quality. When the minimum quality is reached (i.e., -126dBm for R1, -114dBm for R2), the MR transmits the TC to the answering lander.

(R1 = approx 8 kbps) (R2 = approx. 128 kbps)

- d. After detection of the TC, the lander completes sending the last Viterbi pattern sequence, and begin sending the lander telemetry. (see the attached figure)

- e. Loss of signal at the MR terminates the BTTS.

Table 9-2 MR Beacon Subcarrier Frequencies

Telemetry Command (TC)	Request Command (RC)
1376.34 0.002 Hz	RC1: 1484.06 0.002 Hz
	RC2: 1137.78 0.002 Hz
	RC3: 1028.11 0.002 Hz

3. The link margin is 4dB over a 10 minute relay interval.
4. The communication orbiter elevation mask shall be 20° for 60° latitudes, and 5° for 90° latitudes (i.e., ice caps).
5. The Mars Relay can receive on either F1 = 401.5275 MHz or F2 = 405.6250 MHz. The stability of F1 and F2 must be 1×10^{-7} over 1 s, 1×10^{-6} over 1 min., 2×10^{-6} over 15 min., 7×10^{-6} over 15 days, and 1×10^{-5} worse case.
6. Modes
 - a. The MR can communicate with three different landers in the same beamwidth without jamming. The MR will be commanded by uplinked sequence commands (to the orbiter) to select one lander or two alternating landers.
 - b. The available modes are identified in Table 9-3. Three categories of landers are identified: Lander 1 (L1), Lander 2 (L2), and Lander 3 (L3).
 - c. The data rate is selected on the orbiter by sequenced commands. Permissible data rates of 8 and 128 kb/s before convolutional encoding are:

If F1 is used: R1 = 8003 b/s , R2 = 128038 b/s
If F2 is used: R1 = 8085 b/s , R2 = 129345 b/s
 - d. Data rate and carrier frequency are coherently related to each other. The coherency ratio is 3136 for R2 and 3136x16 for R1.
7. Viterbi coding uses a convolutional code of 7-1/2. The modulation is bi-phase L with modulation index of 60% 10%. Worst case losses are: data loss, -1.5dB; carrier loss, -7.8dB. (this coding is optional on the lander telemetry data)
8. Doppler capability is contained in the Mars Relay and may be used for lander location determination.
(all Doppler ranging is conducted using the 16 second BTTS telemetry, accuracy is TBD)
9. The command link for the Candidate 1998 Orbiter is undefined at this time.

Table 9-3. Mars Relay (MR) Modes

Mode #	Lander	Beacon	Data Rate	RF Freq.	Vit. Dec.	Calling Order	Sub.
M1	L1 only	On	R1	F1	On	RC1/TC	
M2	L1 only	On	R1	F1	Off	RC1/TC	
M3	L2 only	On	R1	F1	On	RC2/TC	
M4	L2 only	On	R1	F1	Off	RC2/TC	
M5	L1/L2 alt.	On	R1	F1	On	RC1/TC-RC2/TC etc.	
M6	L3 only	On	R1	F1	On	RC3/TC	
M7	L3 only	On	R1	F1	Off	RC3/TC	
M8	L3 only	On	R2	F2	On	RC3/TC	
M9	L1/L2 alt.	On	R1	F1	Off	RC1/TC-RC2/TC etc.	
M10	L1/L3 alt.	On	R1	F1/F2	On	RC1/TC-RC3/TC etc.	
M11	L1/L3 alt.	On	R1	F1/F2	Off	RC1/TC-RC3/TC etc.	
M12	L1/L3 alt.	On	R2	F1/F2	On	RC1/TC-RC3/TC etc.	

M13	L3 only	On	R1	F2	Off	RC3/TC
M14	L1 only	On	R2	F1	On	RC1/TC
M15	Test 1	On	R1	F1	On	No modulation
M16	Test 2	Off	R1	F1	Off	NA

9.2 Direct (DSN) Link (direct to earth is not an option for Micro-Met)

A. Capabilities of, and interfaces with, the DSN are described in Deep Space Network/Flight Project Interface Design Handbook, JPL 810-5, Revision D, Volume I (Existing DSN Capabilities). The following additional capabilities are anticipated for use by the MSP Project.

1. Four additional 34m beam waveguide antennas will be built, three at Goldstone and one in Australia. Their X-band operational dates are per Table 9-4.

Table 9-4. New 34m BWG Antenna X-band Operational Dates

Antenna	Location	X-band Receive	X-band Transmit
1	Goldstone	Oct-94	N/A
2	Goldstone	Jun-96	Apr-97
3	Goldstone	Oct-96	May-02
4	Canberra	Oct-97	Oct-97

2. The 70m X-band uplink capability operational dates are per Table 9-5.

Table 9-5. 70m X-band Transmit Operational Dates

Station	Antenna Location	70m X-band Transmit
DSS-14	Goldstone	May-99
DSS-43	Canberra	Dec-99
DSS-63	Madrid	May-00

3. Block V receivers (residual or suppressed carrier modulation, non-return-to-zero (NRZ) and bi-phase)

4. Microsecond accurate telemetry time tagging of packet telemetry received at DSN stations.

5. Full Consultative Committee for Space Data Systems (CCSDS) convolutional/Reed-Solomon decoding capability.

6. Stream splitting and data routing using CCSDS packet telemetry formats.

B. X-band shall be used for Earth-to-Mars uplink and Mars-to-Earth downlink. The transmissions shall use 34m and/ or 70m DSN antennas in the Category B allocation per Table 9-6.

Table 9-6. Category B Mission Frequency Allocations

X-band
 Downlink: 8400 - 8450 MHz
 Uplink: 7145 - 7190 MHz

AND OF SENSORS MARS

(Provided by David Catling, August 22 1995)

(Abbreviations: PCB = printed circuit board, PRT = platinum resistance thermometer, TCO = thermal coefficient of offset, TCS = thermal coefficient of sensitivity)

1. CURRENT DEVELOPMENT STATUS OF PRESSURE SENSORS

The operation and theory of the sensors has been established and possible interface electronics has been investigated. Both components of the sensor package, i.e. (1) the transducer and (2) the electronic interface, would benefit from further development. Some key issues are (a) reducing the temperature dependence of the pressure transducer measurement caused by mounting stress, (b) monitoring the transducer's long-term drift, and (c) addressing the power budget and space-worthiness of the interface electronics.

2. ISSUES REQUIRING FURTHER DEVELOPMENT WORK

Spare prototype transducers are available as bare chips which require mounting. The interface electronics will be rebuilt and improved.

2.1 Transducer development:

(1) the mounting stress will be reduced (and hence TCO) by experimentally evaluating the effect of different mounts on the thermal sensitivity of devices. A way of mounting the sensors suitable for spaceflight will be finalized as a result of this investigation.

(2) demonstration sensors will be calibrated with the interface circuit

(3) measurement will be made of the long-term drift of (a) the transducer chip and (b) the sensor package (chip + interface electronics)

2.2 Interface electronics development:

The circuit developed thus far would benefit from some simplifying changes which will reduce the number of components and lower the output drift.

3. PROPOSED MEASUREMENTS

3.1 TRANSDUCER CHARACTERIZATION

To evaluate the response and temperature dependence of the sensors, the following measurements will be made:

(a) Sensitivity and repeatability:

the capacitance variation with pressure, i.e. pF/mb, will be measured over a range from 1000 mb to 10^{-5} mb and back again. The sensor must be held at a fixed temperature (± 0.1 K) so pressure readings are independent of any temperature fluctuations and their effect on sensor output. Over 0---20 mb, readings will be taken over intervals of 2 mb or less. Static readings will be taken, i.e. the system would be

closed off from pumps/ gas feeds at a particular pressure for each C vs. P point. This will ensure that reference pressure measurement and sensor measurement are equal.

(b) Temperature coefficient of offset (TCO) and of sensitivity (TCS):

measurement of the capacitance of the sensors under high vacuum (i.e. "zero" pressure) as the temperature is increased/decreased will give the TCO. Pressure-capacitance curves at fixed temperatures will indicate the TCS.

3.2 INTERFACE CIRCUIT CHARACTERIZATION

Electronics based on a simplified version of the author's previous design will be breadboarded and tested for functionality. This simplified circuit will consist of a few chips and 30 passive components. Small capacitance variations can be simulated using ceramic (NPO dielectric) capacitors which have zero thermal coefficient specification.

Electronics will be transferred to a PCB to ensure a good ground plane for low noise measurement of small capacitance variations. The PCB will be configured to allow pressure sensors on the board so that the sensor + electronic package can be evaluated.

4. SENSOR CHARACTERIZATION - TEST APPARATUS

A small vacuum chamber is under development with capacity for thermal control and monitoring of sensors under test. The chamber will serve the dual purpose of testing individual sensors and the sensor + electronics package. Sensor temperatures are most easily monitored using miniature PRTs. Pressure is referenced to high accuracy baratrons (conventional capacitance manometers).

◀ Back to MET home page.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 28 12:09 1995 PDT

MICRO-MET PROTOTYPE POWER SUBSYSTEM

Date: 19 July 95

By: Clem Tillier

LITHIUM THIONYL CHLORIDE BATTERIES

Lithium thionyl chloride (Li SOCl₂) batteries have the best performance of any primary (non-rechargeable) battery available for purchase. General characteristics that are of interest to a Mars-capable instrument package:

- 3.45 V nominal cell voltage (no need to string lots of cells in series)
- Three times the energy density of Duracells (at low power operation)
- Very long shelf life (10 years)
- Excellent performance over a temperature range that would leave conventional batteries disabled if not permanently damaged
- Extremely flat discharge curve (voltage-time characteristic)

The flip side of this is that they tend to work only for low power applications, since they can't take much power drain; they are also a bit more dangerous to handle.

MICRO-MET BASELINE POWER SPECIFICATIONS

The Micro-Met station concept calls for six D-size lithium thionyl chloride batteries. They are made in this particular size by several manufacturers; here are some performance figures:

Manufacturer:	Yardney	SAFT	Tadiran
Nominal Voltage:	3.45 V	3.5 V	3.6 V
Energy Capacity:	12 Ah	12.5 Ah	13.5 Ah
Measured at:	40 mA	20 mA	2 mA
Temp Range:	-40 to +85 C	-40 to +95 C	-55 to +85 C
Max Current:	N/A	2.5 A	500 mA

The max current rating is somewhat arbitrary. The more current you drain from the battery, the less total capacity it gives you. The energy capacity rating is given for currents on the order of a few milliamps; in the high current regime (a few hundreds of milliamps), efficiency is approximately halved for every 2.5 fold increase in current.

Energy capacity is measured at room temperature; when the temperature drops to about -40, the energy capacity is reduced to about 60% of its original value.

Power Modes

Using the current version of the power budget and assuming a six-battery configuration, where the batteries are connected in parallel and give a system voltage of 3.45 V:

Mode	Sleep	Measure	Transmit
Power	6 mW	400 mW	4600 mW
Current (total)	1.7 mA	116 mA	1333 mA
Current (per cell)	0.28 mA	19.3 mA	222 mA

The energy total for a transmit day is only 10% higher than otherwise.

Electrode Passivation

Lithium batteries owe their long shelf life to a film of LiCl that forms on the anode and prevents leakage. This phenomenon is called electrode passivation, and it can be a concern when starting a battery after a long period of storage. The film greatly increases the internal resistance of the battery, to the point that the terminal voltage can take a serious dip if much current is drawn. This effect only lasts on the order of ten seconds, enough time for the coating to be burned off.

Tadiran gives some information on the dynamics of initial discharge. The effect lasts about ten seconds, and the terminal voltage drops to a value depending on how much current is being drawn. If the voltage drops below 2.5V, the battery cuts off and comes back on line when the voltage can exceed 2.5V.

Current Draw (per cell)	30 mA	60 mA	250 mA	500 mA
Transient Min. Voltage	3.4 V	3.0 V	< 2.8 V	< 2.5 V

Passivation occurs only when the cell is not used at all for an extended period. If we were to turn on and transmit immediately, the voltage would drop to a level dangerously low for the CMOS electronics, which usually bottom out below 3 V. However, Tadiran told me that current draws of a few microamps were sufficient to avoid the phenomenon; this should put us out of the danger zone.

Buffered Supply?

Initially, we thought it would be necessary to back up the lithium batteries with a second power supply (using a capacitor or secondary batteries) to take up the transients. The performance benefits of this are marginal, since only 0.3% of the energy drawn from the power system is used under high current operation. At about 250 mA, most lithium batteries have their energy efficiency halved, so there is a net loss of 0.3% of the battery's total energy content. This could be avoided using the buffered design, but clearly the benefits are negligible. Not only would such a system be complicated to design, but lithium batteries of the size we plan to use can easily handle the current transients.

Longevity

A quick calculation shows that 6 D-size cells would last on the order of 562 sols, or not quite enough to last a whole Martian year. This uses the conservative figures in the current power budget; if it is really a problem, more cells must be added.

AT -40°C

PROTOTYPE POWER SYSTEM

The prototype station's power system should be as close as possible to the flight system. Since we are using a terminal node controller and a handheld radio for communications, we will have to simulate the real system with dummy loads, sized according to the power budget.

General Characteristics

We would like to simulate the flight system as best we can; this dictates the choice of six D-size lithium thionyl chloride cells. I suggest we wire them in parallel, for two reasons:

- 3.45 V bus will drive CMOS quite nicely, and keep power consumption (proportional to V^2) to a minimum.
- The batteries will stabilize each other's discharge curve, making the output voltage very stable in time

The only drawback might be for D. Catling's sensors; he had originally requested up to 4 V. Hopefully 3.45 is OK. Another concern is that the battery terminal voltage will drop with decreasing temperature; at -40 degrees, it's down to 2.9 V. Is this a problem we should worry about?

Regulation

Since lithium thionyl chloride batteries have such a flat discharge curve, I see no reason to regulate the voltage unless there is a voltage-dependent calibration somewhere in the system. Can we identify any such instances?

Dummy Loads

The dummy loads will not present a technical challenge; they can be made from ceramic resistors, available cheap at Haltek.

TNC Interface

Interface with the TNC is RS232. We had agreed to supply the TNC power separately, but the CPU end of the interface still needs to drive the +5, +15 and -15 volt RS232 signals. There are chips available to do this, using "on-board flying capacitor voltage converters" to generate the necessary negative voltage from a single +5 volt supply. (Texas Instruments: MAX-232 and LT1130 series, LT1080)

Meeting, 30JUN95

Hello,

I'd like to review the main points from the meeting today, including the tasks assigned to each of us, then suggest a schedule for our next meeting.

1) Today's meeting agenda:

- discuss schedule for summer research project
- discuss/clarify Micro-Met design details
- provide supporting doc's from the Mars Surveyor RFP
- schedule meeting for next week

2) Tasks:

- Brian, Mike and Clem will review/revise and complete the rough schedule presented today. The basic outline was accepted (approx. one third time devoted to each of design, assembly and test/demonstration). Major research project milestones will include presentations at NASA/Ames and the InterMarsNet conference paper.
- Brian, Mike and Clem will map the Micro-Met functional block diagram (as provided by Steve) into the capabilities/experience of the Small Sat lab. This will help those of us from Ames to understand how best to proceed this summer.
- Steve will provide a mission statement document to define the mission goal, design drivers and identify significant design trade-offs (for example, power supply, data handling logic options etc.)

3) Next meeting date:

The agreed upon schedule for the next meeting is;

Wednesday, July 5, 2:00 pm Stanford University Durand Building, Timoshenko Room (2nd floor)

The meeting will focus on the science sensors and interface electronics as developed by David Catling (note to Bob Haberle, can you forward this to David Catling?). We will also discuss each of the tasks defined above.

See you all there.

Steve M.

◀ Back to MET Meeting Minutes.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 14 18:58 1995 PDT

Meeting, 05JUL95

Hello,

I'd like to remind you of our next meeting and to review a few notes from the meeting yesterday.

First off, our next meeting -

Wednesday, July 12, 2:00

Durand, Room #166

Topics: Power and Battery data (Steve M.)

Micro-Controller details (Michael, Brian and Clem)

Schedule (Clem etc.)

Now, a few notes from yesterday (in no particular order) -

- 1) Temperature sensors will be required for pressure sensor calibration (may be able to record at 7 bits versus 8). Memo, page 3. - David C.
- 2) The revised measurement requirements (memo, page 2) are; accuracy at least 0.2% precision at least 0.1% (David C. notes that the goal is resolution to 0.01 mbar with a range from 0 to 10 mbar)
- 3) The memo (page 2) should read 25 measurements per day, not 5
- 4) A baseline sampling plan was agreed upon;
 - sensors on for 10 seconds, take 20 measurements from each
 - store this data in CPU buffer memory
 - "sensor failed" logic may use mean and standard deviation of the 20 measurements from each sensor to detect failed sensor and set flag in engineering telemetry
 - time tags (frequency and type) to be determined
 - store mean data (1 for pressure, 1 for temperature) into long term memory
- 5) The sensor interface (as shown on the functional block diagram in the memo) is baselined as an analog voltage signal, 0 to +4 volts. 12 bits for pressure, 8 bits (or less) for temperature. - David C.
- 6) The electrical power system design will be "flight like". It will use LiSOC12 (Lithium Thionyl Chloride) batteries coupled to either a NiCd batteries or a capacitor for surge power. This system will provide power for "flight like" loads (may require "dummy" electrical loads). The TNC (terminal node controller), or other lab support systems, will be powered independently.
- 7) The pressure and temperature sensors will be for terrestrial applications. Mars environment sensors may be used later in the project (time permitting). Pressure sensors will be designed by David C., the temperature sensors are to be determined.
- 8) The communications system will use a terminal node

controller. The demonstration will aim towards a WWW page hookup through the Stanford ground station instead of the potential WeberSat orbital relay.

That's all for now.

Steve M.

P.S. Bob Haberle, can you pass this on to David?

◀ Back to MET Meeting Minutes.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 14 18:58 1995 PDT

Meeting, 12JUL95

Hello all,

A few notes from yesterday's meeting and then a copy of the design review announcement that will be circulated at Ames.

Notes:

- 1) Schedule: Clem will e-mail a revised edition to each of us.
- 2) Design review: To be held at Ames next Friday (see announcement below). The review will focus on the electronics and their functions. A brief mission (and research project) introduction will be given by the students. The review will be scheduled for one hour. The room will be reserved for two hours (total) to allow for discussion.
- 3) Steve Merrihew will meet with Brian, Clem and Michael on Wed., July 19 for a dry run of the design review.
- 4) Steve Merrihew is pursuing long term (approx. three months) visitor badges for the Stanford team.
- 5) Science Instruments: David Catling currently has bare sensor chips, these need to be mounted and calibrated. The interface electronics (capacitance to voltage) are designed, but not assembled. The final design of the interface electronics is to be determined. The baseline interface requirements are a 0 to +5 V analog signal. Temperature sensors may be Platinum resistors (coupled with interface electronics) or a commercially available sensor as used by the SSDL.
- 6) The Micro-Controller Unit (MCU) has been purchased, delivery is expected by early next week. The MCU supports 12 bit A/D conversion and additional RAM. This MCU will be used to develop a more "flight like" system later on.
- 7) Handouts included the following:
 - MCU requirements (Michael Hicks).
 - Lithium Battery data; Mass, Volume, Power and Energy budget spreadsheets; Mars Surveyor 1998 lander mission Proposal Information Package (Steve Merrinew).
- 8) Clem has set up an initial WWW page for the MIncro-Met project. Go take a look. Link to it from the SSDL page. The address is

<http://aa.stanford.edu/~ssdl/>

The announcement:

What: Micro-Meteorology Station Prototype Design Review
Where: Building 244, Room 209
When: Friday, July 21, 10:00 am

Work to be done:

A) The external beacon will be implemented via the TNC and not via an external beacon tone as originally planned. The TNC beacon provides the functional demonstration with reduced impact on the schedule.

B) The electrical power system will be simulated by assembling the batteries into a set of six and running these through a simulated power cycle. This simulated power cycle will result from a careful accounting of the flight-like hardware component power requirements by the Stanford team and the mission profile presented by NASA Ames. This test will be conducted at hot and cold temperatures.

3) NASA/Ames CDR presentation outline:

I. Introduction -- Steve Merrihew

What is the Micro Met Mission?

Where does the Stanford study fit?

II. Schedule and Test Plan review -- Stanford

Where are we now?

What has changed and why?

How will we know when we are finished?

How will we demonstrate that we are finished?

III. Technical presentation of each subsystem -- Stanford
details, details, details!

IV. Work remaining -- Stanford

What needs to be done?

What are the problem areas?

Note, a demonstration may be performed, but it is not planned at this time.

That's it. See you Tuesday.

Steve M.

◀ Back to MET Meeting Minutes.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 14 18:58 1995 PDT

MICROMET PDR NOTES

These are Steve Merrihew's notes on the Preliminary Design Review held by Brian, Mike and Clem on 21 July at NASA Ames.

Hello all,

Here are my notes from the Micro-Met PDR meeting held this past Friday (July 21) at NASA Ames. This report has been expanded from the previous notes (June 25, 1995) by adding a task or answer after each concern/question.

I feel that the meeting went well. I was pleased to see that we had technically minded people in the audience to test us on the details of the design. In the future we will have to be more complete in our introduction so that we are sure that the audience understands both the Micro-Met mission (from the Ames perspective) and the Micro-Met summer project (the Stanford team tasks). The confusion was admittedly complicated by the late arrivals of some of the audience. There's not much we can do about that!

Micro-Met team:

Ames - Bob Haberle, David Catling, Larry Lemke, Steve Merrihew
Stanford - Bob Twiggs, Brian Engburg, Clem Tillier, Michael Hicks

CDR Attendees:

Ames - Doug O'Handley, Jeff Ota, Bob Hanel
SkyWatch - Gary Langford, Joe Zott
Consultant - Robert Zimmerman

My notes (in the order of the presentation):

1) Introduction (Clem) - As noted above, we should spend more time with the introduction in future presentations. The intro. should include both Ames and Stanford personnel to help clarify the Micro-Met mission and summer project plans.

--> Future presentations will include Micro-Met mission presentation from Ames personnel, including rationale for measuring pressure only. Pressure is the fundamental surface measurement for atmospheric science. Surface pressure, combined with orbital atmospheric temperature measurements (atmospheric sounders), enables the determination of the three dimensional wind profiles.

2) Micro-Controller Unit (Michael) - Questions were raised about the tradeoffs between EEPROM and standard RAM. We should conduct a trade study of this, with total energy and peak power as the primary decision criteria. A question was asked about the timer circuit clock speed (from Joe Zott), this may have impact on total energy requirements.

--> Michael Hicks will perform this study as all of the required data is presently available.

3) Science sensor resolution (David) - While not a part of the formal presentation, the validity of a 12 bit pressure measurement at Mars was questioned by Robert Zimmerman. Concerns regarding measuring absolute pressure with sensor drift may make a 12 bit resolution unnecessary (a 10 bit resolution may be more appropriate given the possibly limited

absolute accuracy of the measurement). The 12 bit measurement is a science requirement at this stage, so this issue needs to be clarified. Perhaps a long term sensor test plan can be proposed to address the stability of the sensors.

--> A 12 bit resolution for the measurement of pressure is a science requirement. This resolution is required to detect weather fronts in the martian atmosphere. The current sensors (as developed by David Catling) have a sensitivity of approximately one pico-farad per milli-bar which supports the 12 bit resolution requirement. Temperature sensitivity and noise issues will be addressed in a long term test program (note that this sensor development is outside the scope of this summer's Micro-Met prototype project).

4) Communications (Brian) - The delineation between "flight-like" and the laboratory communications systems (the UHF Mars Relay and the TNC) caused some confusion (although I thought the presentation was clear). Also, we need to identify the components required in the TNC supported lab comm. system.

--> The TNC system has been delivered. The delineation between "flight-like" and laboratory equipment will be made more clear once the prototype is demonstrated. Note that the use of the TNC's is to simplify the implementation of the prototype communication system and is not a part of the "flight-system" design.

5) Electrical Power (Clem) - We need to identify the sleep power requirements (RAM and clock) as this has a huge impact on the overall energy requirements. There was concern about the safety of D-cell LiSOC12 batteries, C-cells are a safer alternative for work in the laboratory (Gary Langford). Is this a suitable substitute for our study? Clem's analysis suggests that we do not need a buffered power system (using either a NiCd or a capacitor) to provide surge power during communication periods. I'd like to see a lab test of this, focusing on the cold case (Tmin approx = 230 K) (as suggested by Joe Zott).

--> The LiSOC12 batteries will be purchased in the D-cell configuration and all safety protocols will be met as indicated by the supplier (this is according to SSDL practice). The integrated power system will be tested at cold temperatures. The steady state power requirements will be carefully tracked (Clem Tillier is the lead on the electrical power system).

6) Question and Answer period:

A) What is the test plan? What are you trying to show? How do you know when you are finished? (from Gary Langford and Joe Zott). I (Steve M.) will take this task and will have a draft plan for the meeting later this week.

--> The high level test plan has been developed (dated 07/26/95) The implementation of the test plan, including the writing of the test report, is the responsibility of the Stanford Team. This report is due in mid-September.

B) Radiation environment (deep space versus on the surface of Mars). This question relates primarily to the actual Micro-Met mission, however it would be valuable to identify the radiation tolerance of our

prototype components. This task is assigned to Michael, Clem and Brian.

--> The final design report (to be written by the Stanford team) will define the environmental specifications of the prototype hardware. These specifications will be compared to the anticipated mission environment as supplied by NASA Ames. The objective is to determine which commercially available components can operate within the mission environment.

C) Surface impact and high g tolerance of electronic components. As with the previous question, primarily a flight mission issue. I (Steve M.) will take this task to identify how commercial components are "ruggedized".

--> These specifications (as determined by NASA Ames) will be compared to the anticipated mission environment as supplied by NASA Ames. The objective is to determine which commercially available components can operate within the mission environment.

That's all.

Thanks to Brian, Clem and Michael for staying up late to finish the presentation. Now we can get to work on the hardware!

Steve M.

◀ Back to MET home page.

*Maintained by: MET team
Send email to: ssdl@aa.stanford.edu
Last modified: Jul 28 14:57 1995 PDT*

Meeting, 23AUG95

Hello all,

After a long delay, I am returning to the ritual of posting meeting minutes to our little group (and the world via the Web).

Today (Wednesday, August 23), Brian, Clem, David and myself met to review and prepare for the upcoming CDR to be held at NASA/Ames (Tuesday, Aug 29, 1:00, Building 244, room 209). Topics for today's meeting were:

- 1) Review current status of the prototype design
- 2) Identify work remaining and schedule impacts
- 3) Plan the NASA/Ames CDR presentation

The following provides a brief review of these topics.

1) Status:

Clem and Brian presented a summary of the hardware and software status. Briefly, the various segments of both the hardware and software work independently, but not as a unified system. The basic problem appears to be in the implementation of the micro-controller interrupts. These interrupts are required to initiate the data collection and communication events autonomously on the Micro-Met prototype station. The micro-controller evaluation board (the "NMI board") and associated hardware are all on hand, except for a low power clock circuit. The software is essentially all written and is not expected to be an impact on the schedule. The design of the second phase hardware using a reduced number of independent components interfaced without the NMI board does not appear to be feasible in the time remaining. The second phase hardware had been an option in the project as the NMI board based prototype will satisfy virtually all of the Test Plan functional requirements. Without the custom second phase design the electrical power subsystem cannot be fully implemented (see the following section for a electrical power system plan). The implementation of the external beacon (the laboratory simulation of the Mars Relay orbiting beacon) is not complete, see the following section on work to be done for details. So, the "Hot" List for hardware and software is:

- A) Interrupt routines on the NMI board
- B) Electrical power subsystem design and test implementation

2) Work to be done:

The above mentioned problem areas have caused us to modify the schedule. The new schedule is listed here (please see the Web page for the complete schedule):

August 29,	NASA/Ames CDR
September 1,	Design/Test Status review at Stanford
September 8,	Test Status review at Stanford
September 15,	Documentation review at Stanford
September 18,	Documentation Due

Why: Bob Haberle, Larry Lemke, David Catling and myself would like to invite you to attend a design review for the Micro-Met Station prototype research project. The Micro-Met mission, developed here at Ames, is designed to place 16 or more long lived stations on the surface of Mars for global atmospheric science. This summer's Micro-Met Station prototype research project is the result of a Joint Research Investigation (JRI) grant to the Stanford University Small Satellite Development Laboratory from the Space Projects Division, Advanced Studies branch. The goal of the summer project is to design, develop and demonstrate, through rapid prototyping techniques, the electronic subsystems of the Micro-Met station.

Please join us as the students provide a review of their design and then present the initial hardware elements for the electronic subsystems.

See you there.

Steve Merrihew

That's all for now.

Steve M.

◀ Back to MET Meeting Minutes.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 14 18:58 1995 PDT

Critical Design Review, 29AUG95

Hello,

It looks like we had a successful CDR at Ames. Congratulations to the sleep deprived Stanford team for pulling it all together in time!

In this post I'd like to:

- 1) Pass on the notes that I took during the CDR
- 2) Discuss where we are now and what we should push on to finish
- 3) Review our upcoming schedule

-->> Note that we will have a meeting this Friday, September 1 at Stanford (3:00, Durand room 166 (the Micro-Met lab)). We will review the CDR and update the status of the design and test program.

On to the details --

1) CDR Notes:

I felt that we did a better job of introducing the Micro-Met program and the context of the Micro-Met Station prototype project. It may have been a bit rushed (hence the questions about the mission science), but I wanted to leave lots of time to the technical presentation. The organization of the presentation was improved as well, including the format of the charts.

CDR audience questions -

A) Software and operations: Why not perform temperature calibrations on the Micro-Met Station to reduce memory and communication requirements? (Joe Zott)

--> The intent of collecting and transmitting both temperature and pressure was to reduce the complexity of the Micro-Met surface station. The calibration of the sensors can certainly be more flexible if performed at earth. Additionally, temperature data may provide engineering and potential science value.

B) Power System: Will the flight-like power system be unregulated?

--> The current plan is to run the electronics directly off the batteries (nominally 3.45 Volts), therefore unregulated. The power system test will provide insight into this capability (cold temperatures are a concern).

C) Power System test: Will the power system test measure the battery temperature as well as the environmental temperature? (Joe Zott)

--> Now that you mention it, yes! This will provide data on the self-warming capability of the batteries.

D) Power: What are the options for reducing steady state power by using low power clocks and memory devices? (Joe Zott)

--> This is a critical task which must be completed for both the power test and the design documentation. A brief trade study of clock and memory options will be performed and documented.

E) Schedule: Will you meet your schedule? (Doug O'Handley)

--> Yes, see below.

2) Where are we now?

Clem has posted my notes from our meeting of August 23. Generally, those notes are current with the exception that the interrupt sequence problems have been solved. We now have a working Micro-Met prototype, albeit with simplified data analysis routines and a as-yet-to-be-demonstrated communications-on-demand capability via the TNC.

My feelings are that the current focus should be on the power system test and the associated analysis of the power requirements for the flight like systems, including identifying low power clock and memory options. These topics will be reviewed this Friday. Once we have progressed through the power system, we can formalize our documentation plans.

3) Schedule:

Here's a re-post of the schedule developed at our last meeting (August 23). All of these meetings are to be held at Stanford.

Sept. 1,	Design/test review
Sept. 8,	test status review
Sept. 15,	Documentation review
Sept. 18,	Documentation due

As you can see, if we can meet this schedule we will have completed all of our functional and documentation requirements by the end of the summer term.

Please check the Micro-Met Web page for additional information,

<http://aa.stanford.edu/~ssdl/projects/micromet>

That's all for now,

Steve M.

◀ Back to MET Meeting Minutes.

Maintained by: MET team

Send email to: ssdl@aa.stanford.edu

Last modified: Jul 14 18:58 1995 PDT